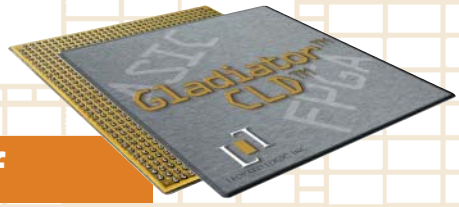


LEOPARD LOGIC, INC.

Product Brief

Gladiator™ CLD™

Configurable Logic Device

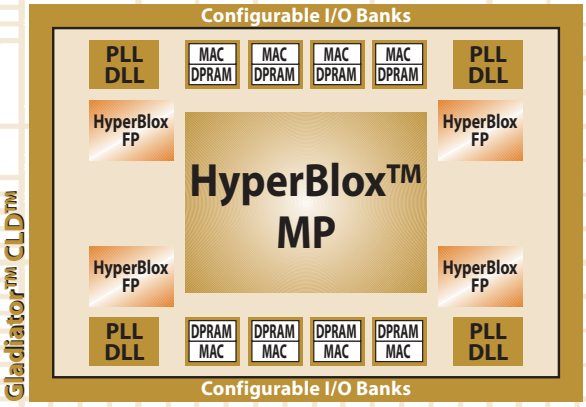
Product Overview

FPGA flexibility combined with ASIC efficiency

The Gladiator CLD family represents the first digital logic device that successfully combines Field Programmable Gate Array (FPGA) technology with hardwired Application Specific Integrated Circuit (ASIC) logic into a new class of configurable logic device.

The basic building blocks of Gladiator CLD are the HyperBlox™ FP and MP fabrics, which are combined with optimized memories, Multiply-Accumulate units (MACs) and flexible high-speed I/Os.

Starting from pre-processed wafers, customers can implement substantial amounts of high speed logic in the mask-programmable (MP) section of the device. After sending the generated configuration data to Leopard Logic, first samples are delivered within weeks. This process is referred to as "marketization" because it transforms the generic device into a customer or market segment specific device. Due to minimum mask and processing requirements, the Non-Recurring Engineering (NRE) costs for this process are an order of magnitude lower than for a traditional cell-based ASIC.



The "marketized" devices can be further customized and differentiated by programming the HyperBlox FP fabric. Like any other SRAM-based FPGA, this fabric allows for an unlimited number of reconfigurations by simply downloading a new bistream into the device, thus offering optimal in-field programmability.

Gladiator CLD Device Family

CLD Device	System Gates	MP Cells	FP Cells	36K DPRAMs	18x18 MACs	PLL DLL	ASIC Gates
CLD1600	1,600,000	16K	1K	16	16	4	200,000
CLD3200	3,200,000	32K	2K	32	32	8	400,000
CLD6400	6,400,000	64K	4K	64	64	16	800,000
CLD12000	12,800,000	128K	8K	128	128	16	1,600,000
CLD25000	25,600,000	256K	16K	256	256	16	3,200,000

Gladiator CLD Highlights

- Unique device combining the flexibility of FPGAs with the efficiency of ASICs
- Rapid time to volume through single-mask configuration
- Field-upgradeable through embedded SRAM-based FPGA
- Available in densities ranging from 1.6M up to 25M Million system gates
- Up to 10 Mbits of embedded memory
- Supports system speeds up to 500MHz
- Flexible I/O options
  - General Purpose I/O: 2.5V, 1.8V LVCMOS/LVTTL, PCI(X), HSTL, SSTL, LVDS
  - DDR/QDR memory support
  - SERDES support
- High-speed MAC units for fast arithmetic and DSP
- Up to 16 PLL controlled clock domains with frequency synthesis and division
- Up to 16 DLL for phase shifting to support interface timing adjustment
- Very low system power requirements
- Compatible with industry-standard ASIC and FPGA design tools

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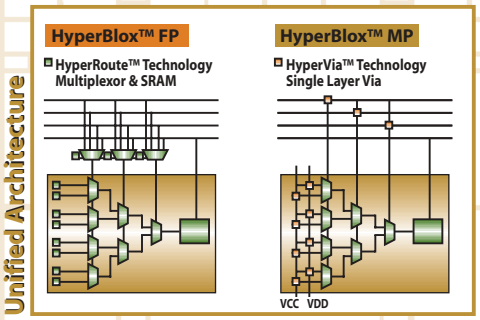
Technology

The HyperBlox FP fabric is based on Leopard Logic's proprietary HyperRoute™ FPGA technology that utilizes the industry's first fully hierarchical, multiplexer-based, point-to-point interconnect.

This technology enables superior speed, utilization, predictability and reliability compared to legacy FPGA architectures.



The HyperBlox MP fabric uses the same logic core cell architecture as HyperBlox FP but replaces the SRAM configuration with a single-layer via-mask configuration, called HyperVia™.

This technology provides significantly higher density, as well as increased performance and lower power.

Design Flow

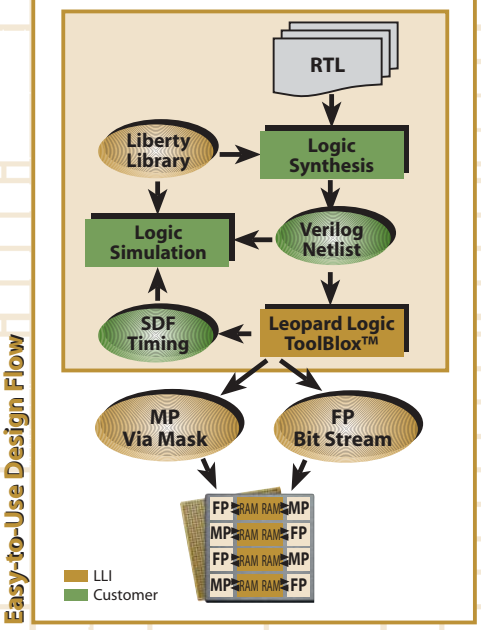
The Gladiator CLD design flow is based on leading industry standard design tools and flows. Combined with Leopard Logic's highly optimized ToolBlox™ back end tools they deliver a significant reduction in implementation and back end processing times. The simplicity of the design flow allows customers to become productive in one day, re-use existing intellectual property, and tap third party resources.

Partitioning between the HyperBlox MP and FP sections of the device is done intuitively. Fixed and stable blocks of the design are mapped into the HyperBlox MP fabric, while high-risk blocks that are still in flux are mapped into the FP fabric.

Designs are quickly and easily synthesized from RTL into a CLD device. Full timing closure is achieved based on accurate timing extraction performed by the user. Bitstreams for the FPGA sections of the device are generated automatically and can be downloaded into the device instantly.

Partitioning between hard (MP) and soft (FP) functions is a snap with the ToolBlox design flow and the unified hardware architecture allows the allocation of design blocks even post-synthesis.

The performance and ease-of use of Gladiator CLD enables customers to instantly tap a vast array of existing Intellectual Property (IP) components from prior designs or third parties. Leopard Logic is teaming up with leading IP providers to assure efficient access to best-in-class, silicon proven IP solutions for its target applications.



Benefits

- Built-in flexibility to meet changing market conditions
- Accelerated time to market due to rapid development and fast turnaround times
- Ease-of use by utilizing existing infra-structure and proven methodologies
- Low risk solution with very attractive NRE
- Ideal for production volumes ranging from 1k to 100k units

Compared to FPGA

- Significantly lower unit cost
- Superior performance
- Higher density
- Lower power requirements

Compared to cell-based ASIC

- Significantly lower NRE
- Field-upgradeable through embedded FPGA
- Rapid design cycle and timing closure
- Faster production time to volume