Introduction to ispMACH™ 4A Family

Introduction

The ispMACH 4A Family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The ispMACH 4A devices offer densities ranging from 32 to 512 macrocells with 100% utilization and 100% pinout retention. The ispMACH 4A Family offers 5V and 3.3V operation.

ispMACH 4A products are 5V or 3.3V in-system programmable through the JTAG (IEEE Standard 1149.1) interface. JTAG boundary scan testing allows product testability on automated test equipment for device connectivity.

All ispMACH 4A Family members deliver First-Time-Fit™ and easy system integration with pin-out retention after any design change and refit. For both 3.3V and 5V operation, ispMACH 4A products can deliver guaranteed fixed timing as fast as 5ns tpd and 182MHz fcnt through the Speedlocking™ feature when using up to 20 product terms per output.

The ispMACH 4A Family offers 21 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flatpack (PQFP), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), Fine-pitch BGA (fpBGA) and Chip Array BGA (caBGA) packages ranging from 44 to 388 pins. It also offers I/O safety features for mixed-voltage designs so that the 3.3V device can accept 5V inputs, and 5V devices do not overdrive 3.3V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition. Tables 1 and 2 describe the Family attributes.

ispMACH 4A Family

- 5.0ns Pin-to-Pin Delay; 182 MHz System Performance
- 3.3V and 5V Versions; Safe for Mixed Supply Voltage System Design
- 32 to 512 Macrocells; 1,250-20,000 PLD Gates
- Speedlocking Performance; Guaranteed Fixed Timing
- Low Power Consumption
- Excellent Routability and Pin-Locking
- Hot-Socketing Capability
- Programmable Bus Friendly or Pull-up I/Os
- IEEE 1149.1 Boundary Scan Testable
- ispJTAG™ In-System Programmable
- Commercial and Industrial Temperature Ranges

ispMACH Development Tools

- ispLEVER™ Systems for PC and Lattice UNIX-Based Design Tools
- Tightly Integrated with Leading CAE Vendors' Tools
- Productivity Enhancing Static Timing Analyzer, Physical Viewer and Explore Tools
- VHDL, Verilog-HDL, ABEL, State Machine and Schematic Entry
- Timing and Functional Simulators
- Comprehensive ISP Programming Tools
- Windows® XP, Windows 2000, Windows 98, Windows NT®, Solaris and Hewlett-Packard UNIX Platforms

ispMACH 4A Overview

The ispMACH 4A Family is ideal for seamless integration into a wide variety of system environments. It provides many features to support system integration: 3.3V support at all densities and 5V support on selected densities; mixed voltage support with 3.3V safety and 5V tolerance; hot-socketing for board-edge and multiple power supply applications; programmable pull-up or Bus-Friendly inputs and I/Os to hold inputs in known states; and JTAG in-system programmability and test for rapid prototyping and efficient manufacturing.

Each ispMACH 4A device consists of multiple PAL® blocks interconnected by a programmable central switch matrix (CSM). Input switch matrices (ISMs) enhance routability by providing input signals with alternative paths into the CSM and output switch matrices (OSMs) assign macrocell outputs to I/O pins. Each PAL block consists of 16 macrocells with 33 to 36 inputs.

The ispMACH 4A devices feature a Speedlocking architecture that provides speed performance as fast as 5ns tpd with up to 20 product terms per output independent of routing and product term usage. Speedlocking delivers

the fastest in-system PLD performance available without requiring time consuming manual design optimization. In addition, the devices also feature a programmable speed/power feature that allows power consumption to be reduced by approximately 50% on logic paths that do not require the fastest possible switching speeds.

ispMACH 4A devices are available in packages from 44 to 388 leads, including PLCC, PQFP, TQFP and BGA configurations. The new BGA packages include Fine Pitch and Chip Array options providing board space reductions of up to 70 percent compared with standard BGA technologies. These packaging options also support logic density migration between ispMACH 4A Family members using a common printed circuit board footprint.

Table 1. ispMACH 4A5 (5V) Family Attributes

Specification	M4A5-32	M4A5-64	M4A5-96	M4A5-128	M4A5-192	M4A5-256
Density (PLD Gates)	1,250	2,500	3,750	5,000	7,500	10,000
Speed: fmax (MHz)	182	167	167	167	160	154
Speed: tpd (ns)	5	5.5	5.5	5.5	6.0	6.5
Macrocells	32	64	96	128	192	256
Registers	32	96	144	192	288	384
Inputs + I/O	34	34	56	70	112	142
Pin/Package	44 PLCC 44 TQFP 48 TQFP	44 PLCC 44 TQFP 48 TQFP	100 TQFP	100 TQFP 100 PQFP	144 TQFP	208 PQFP 256 BGA

Table 2. ispMACH 4A3 (3.3V) Family Attributes

Specification	M4A3-32	M4A3-64	M4A3-96	M4A3-128	M4A3-192	M4A3-256	M4A3-256	M4A3-384	M4A3-512
Density (PLD Gates)	1,250	2,500	3,750	5,000	7,500	10,000	10,000	15,000	20,000
Speed: fmax (MHz)	182	167	167	167	160	167	125	154	125
Speed: tpd (ns)	5	5.5	5.5	5.5	6.0	5.5	7.5	6.5	7.5
Macrocells	32	64	96	128	192	256	256	384	512
Registers	32	96	144	192	288	384	256	576	768
Inputs + I/O	34	34/70	56	70	112	142	160, 192	160, 192	160, 192, 256
Pin/Package	44 PLCC 44 TQFP 48 TQFP	44 PLCC 44 TQFP 48 TQFP 100 TQFP	100 TQFP	100 TQFP 100 PQFP 256 fpBGA	144 TQFP 144 fpBGA	208 PQFP 256 BGA 256 fpBGA	208 PQFP 256 fpBGA 388 fpBGA	208 PQFP 256 BGA	208 PQFP 256 fpBGA

Figure 1. ispMACH 4A Family Packages