



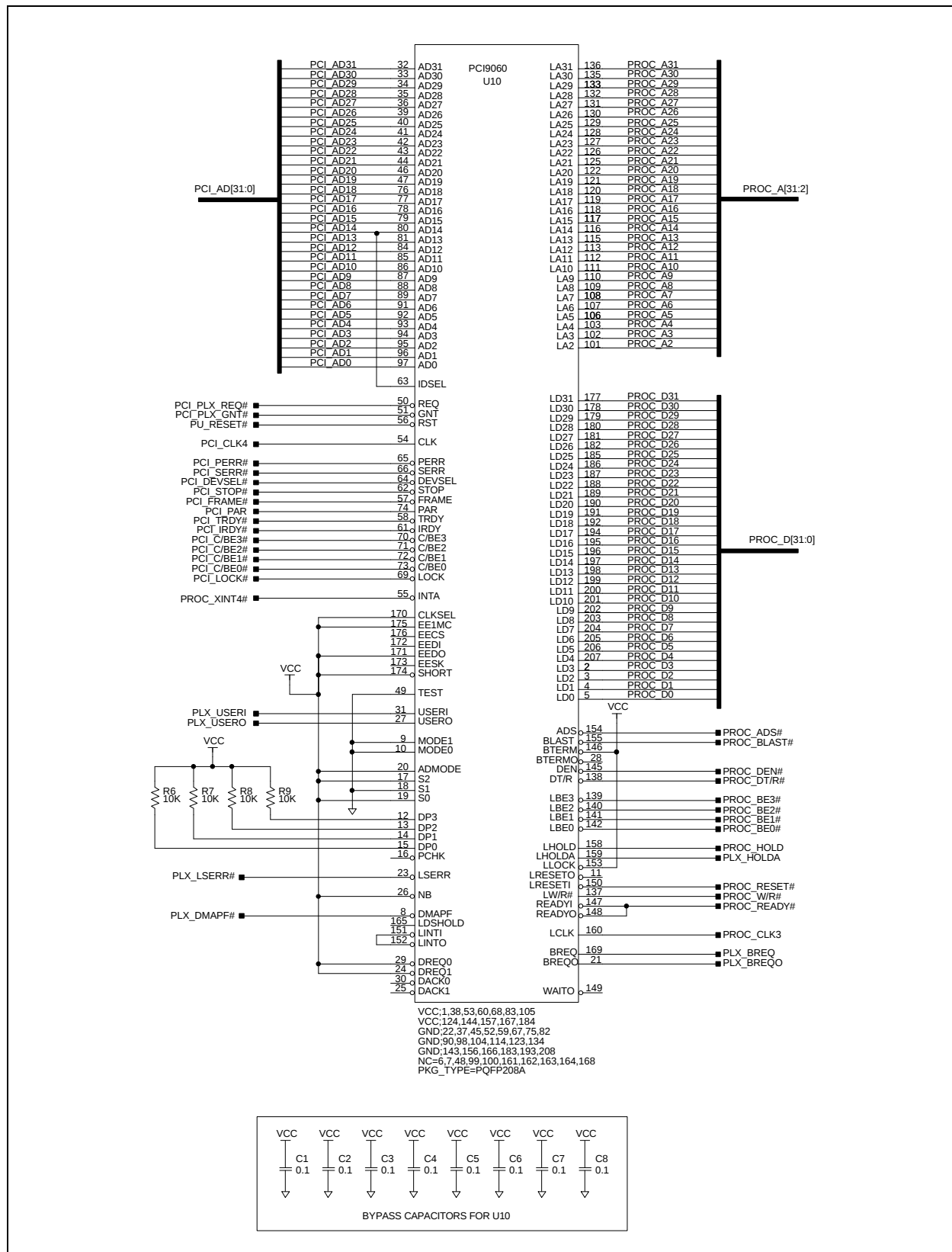
SWITCHED ETHERNET REFERENCE DESIGN SCHEMATICS

Index to Reference Design Schematics

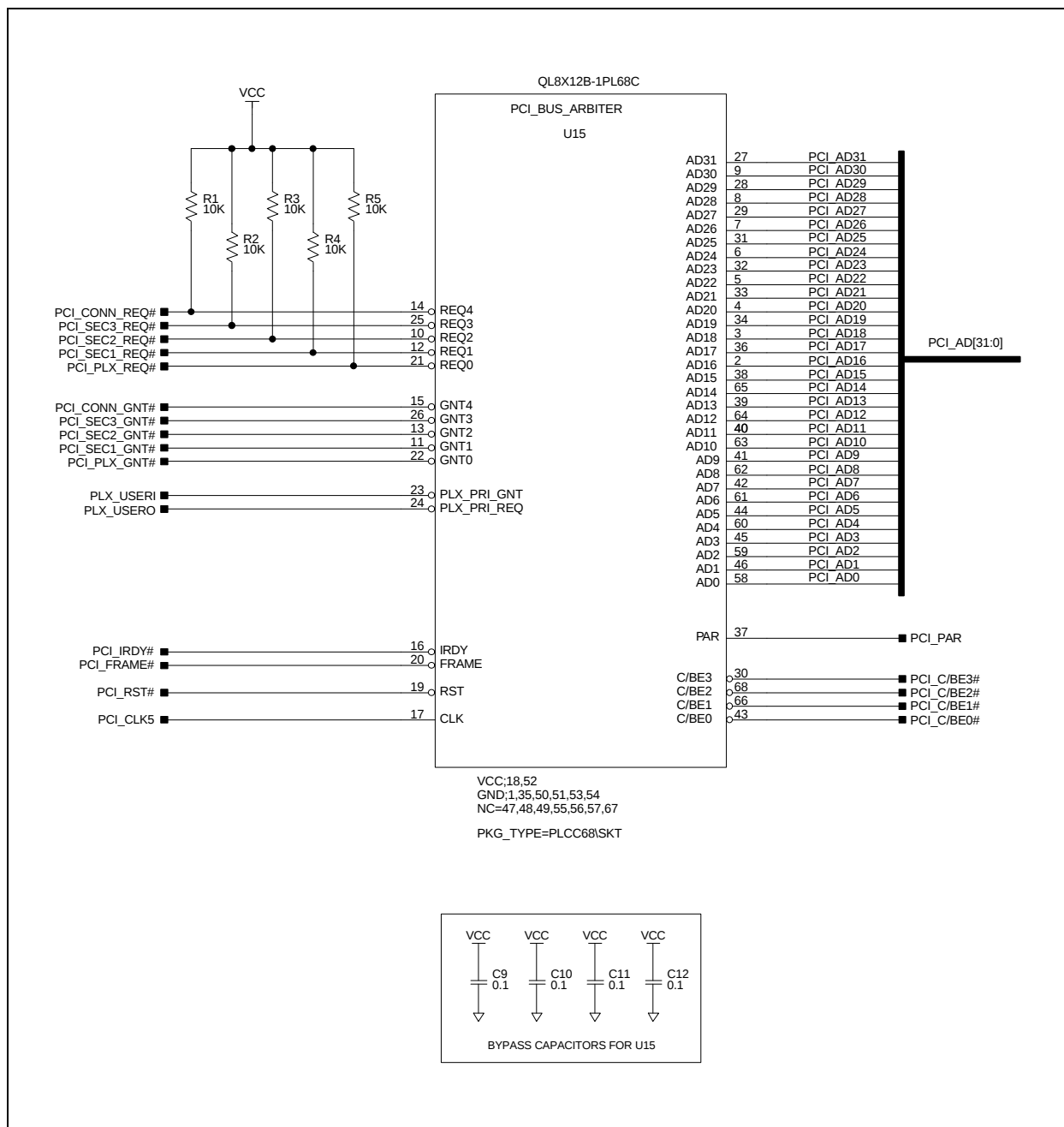
Circuit	Sheets
+3.3V Supply for Processor	3
DIP Switch	25
DRAM Controller FPGA	29
Dual Serial Port (AM85C30)	27
EPROM, 128Kx8	27
Flash Memory	28
Hx Processor	32
Input and Output Ports	25
Input Power Connectors, P25 and P26	33
Jx Processor and Address Latch	31
LED, Processor Fail	2
LED, User LEDs for Debugging	25
LED, Voltage Indicators	2
Misc Logic FPGA	29
PCI Clock Distribution	3
PCI Bus Arbiter	1
PCI Expansion Connector	33
PCI to 80960 Bridge Chip	1
Processor Clock Distribution	2
Processor DRAM SIMM Sockets	30
Power Up Reset	2
Serial EEPROM	25
Serial Port Driver/Receivers	27
Slow Data Bus Transceiver	26
VPP Switch (for Flash Programming)	3

NOTE: The reference design schematic was originally scaled for printing on B size (11"x17") paper. In order to incorporate the drawings into this document, it was necessary to partition some of the sheets, resulting in "a" and "b" sheets. For example, Sheet 2 of the original drawing is shown on two sheets in this document identified as sheets "2a" and "2b".

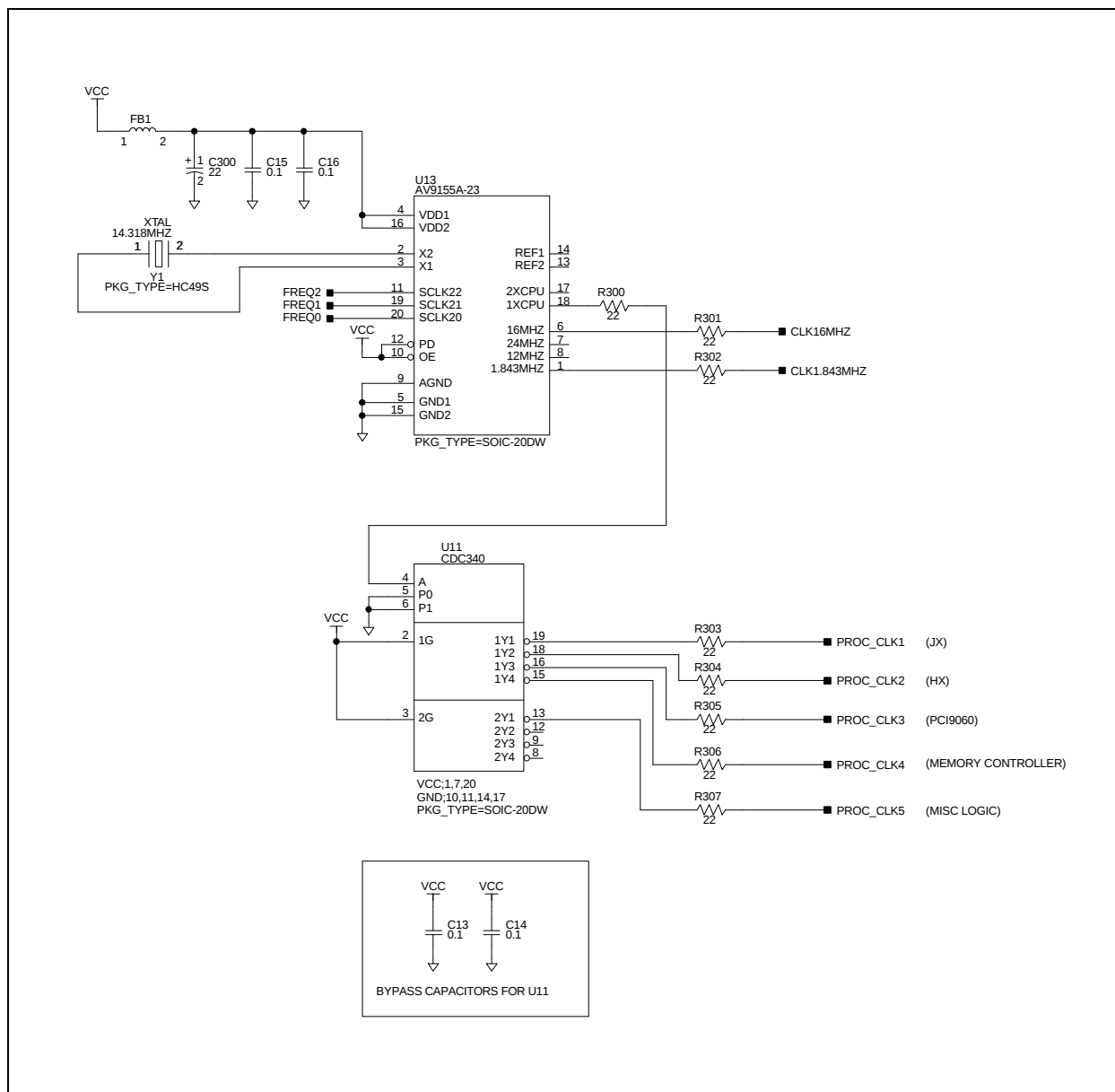
Note that it was necessary to create "a" and "b" sheets for only about half of the original schematics.



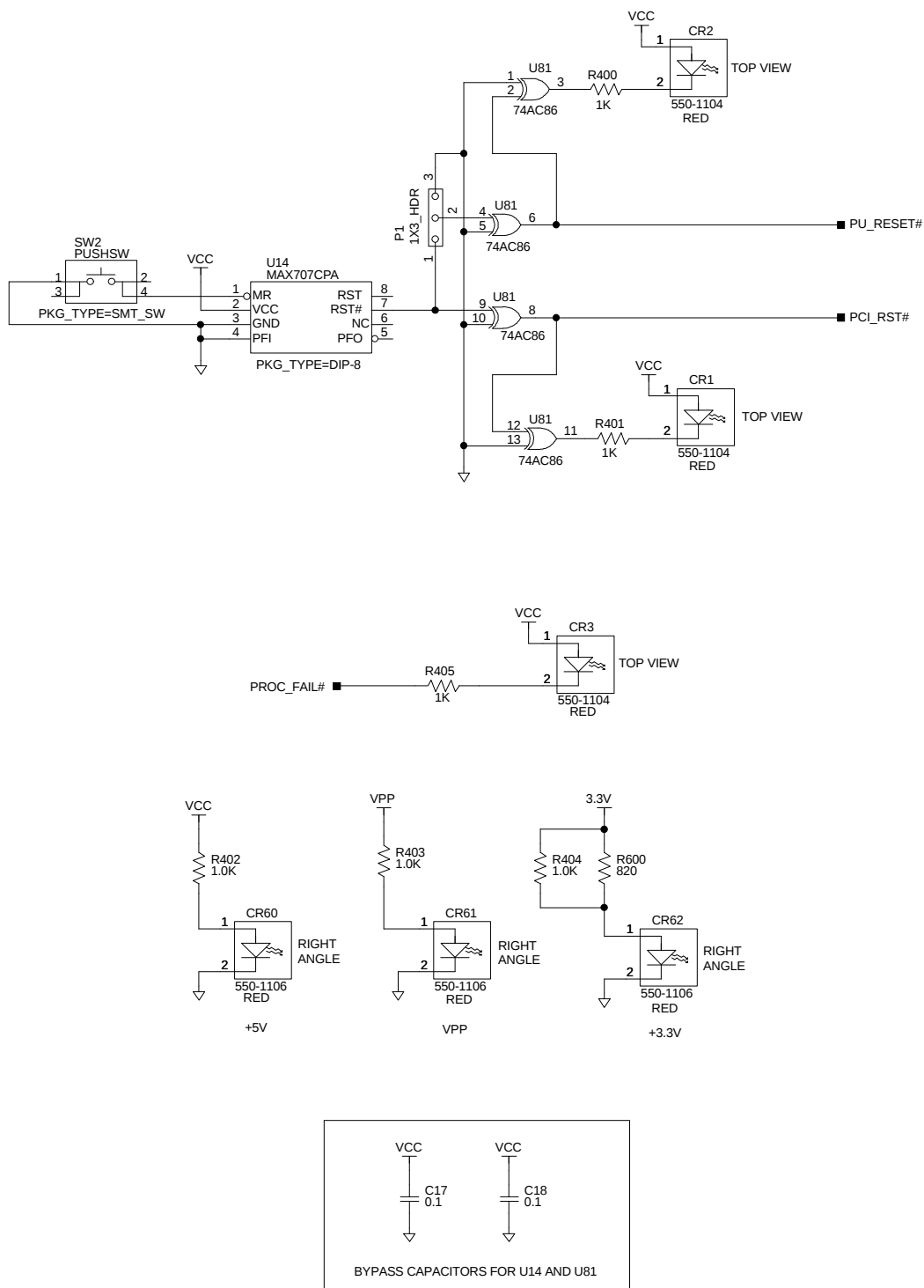
Switched Ethernet Reference Design—Sheet 1a



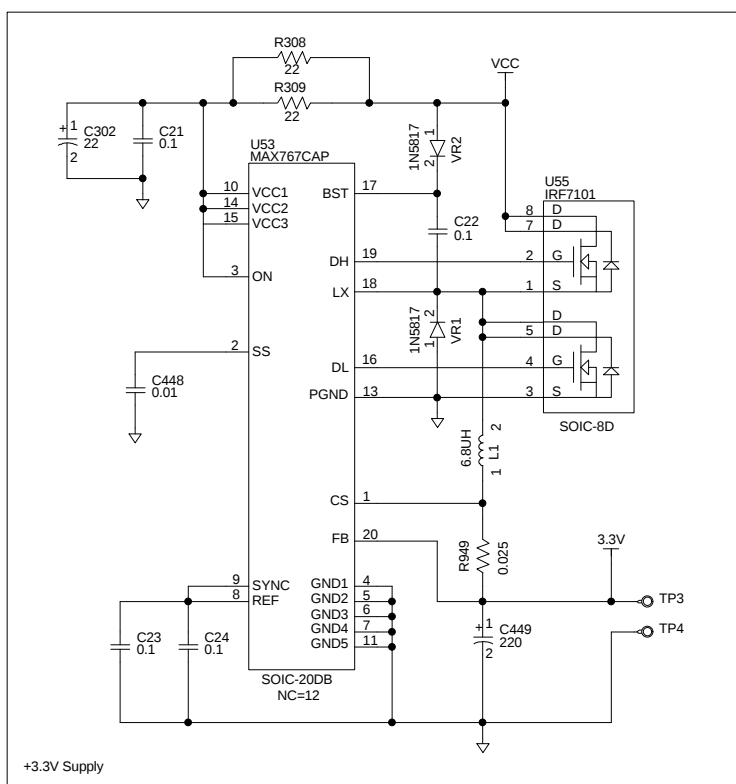
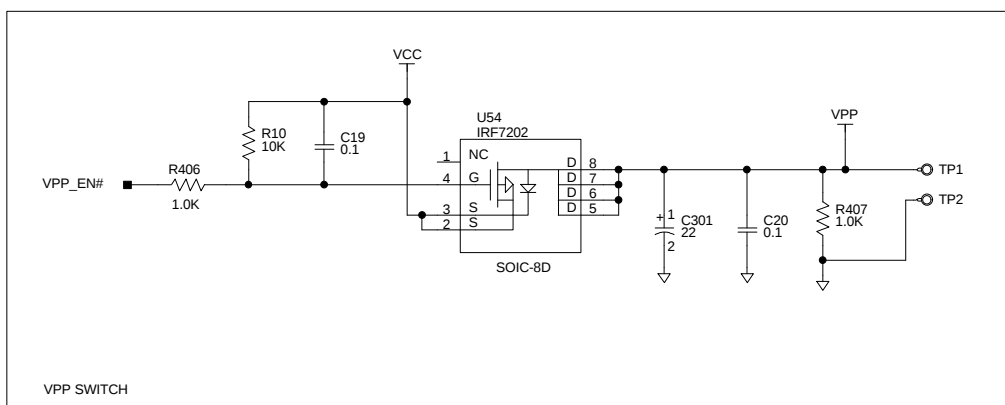
Switched Ethernet Reference Design—Sheet 1b



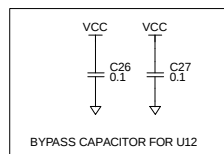
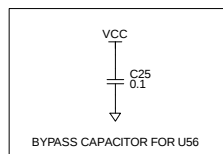
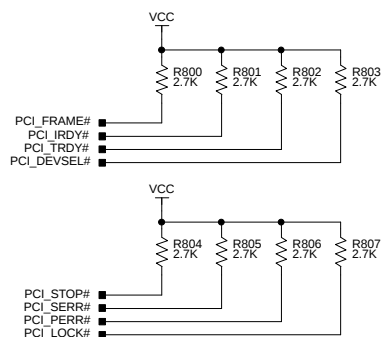
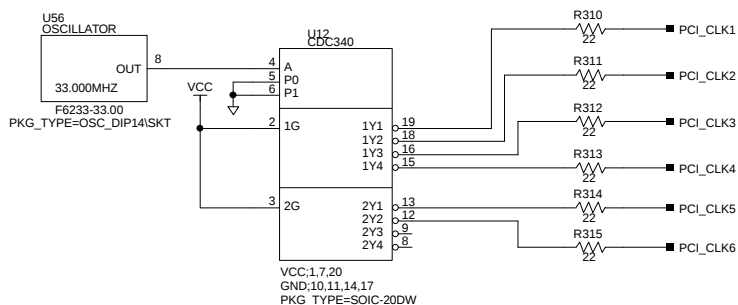
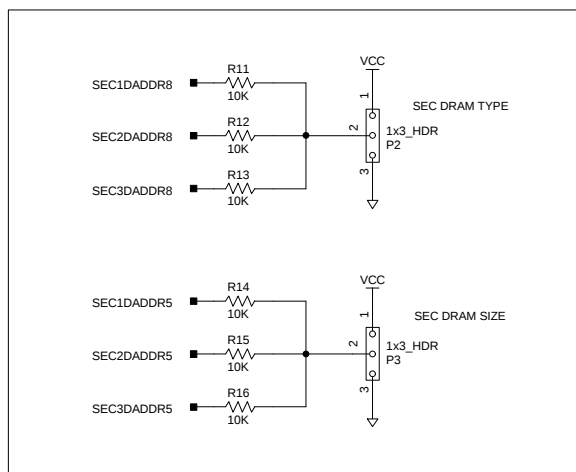
Switched Ethernet Reference Design—Sheet 2a



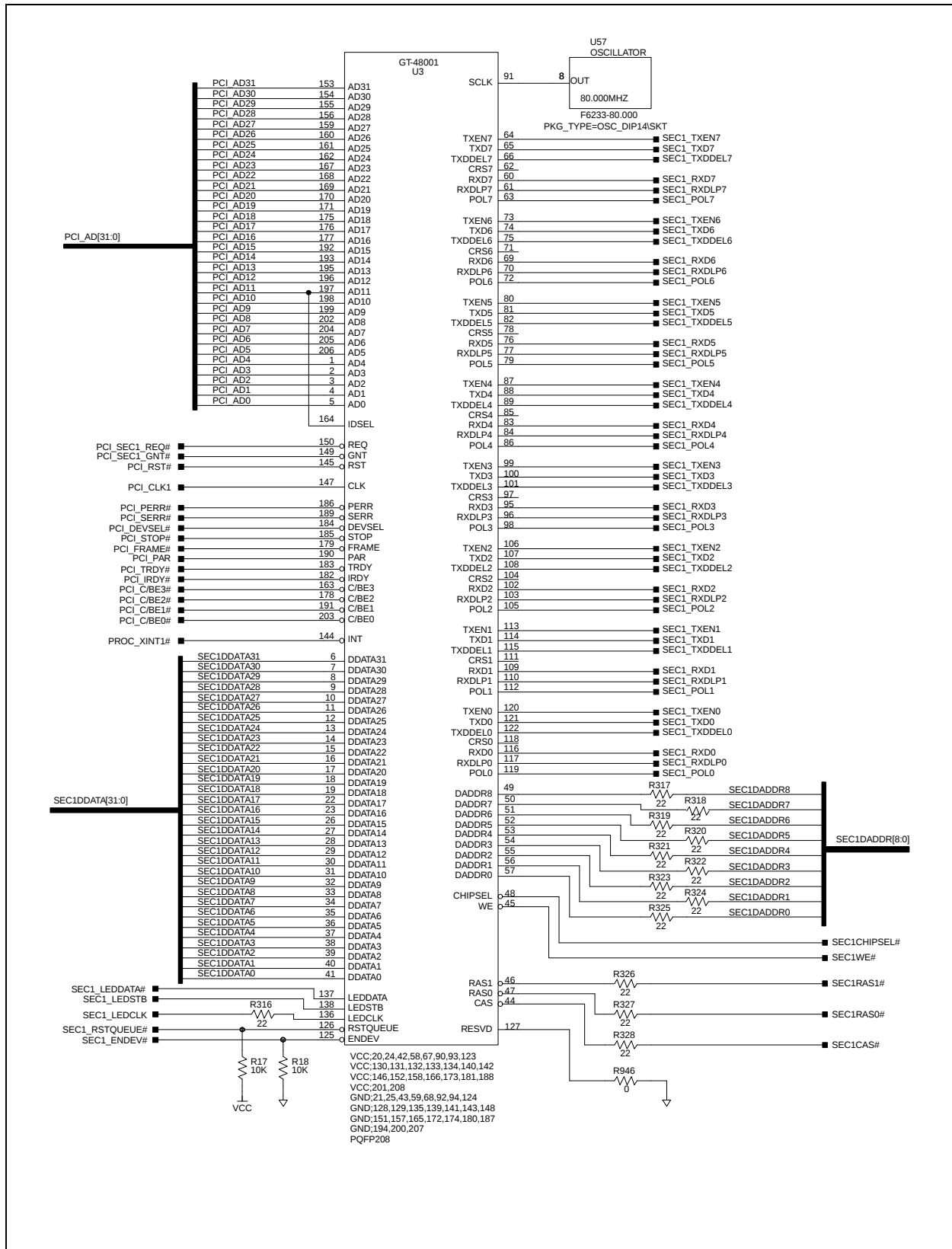
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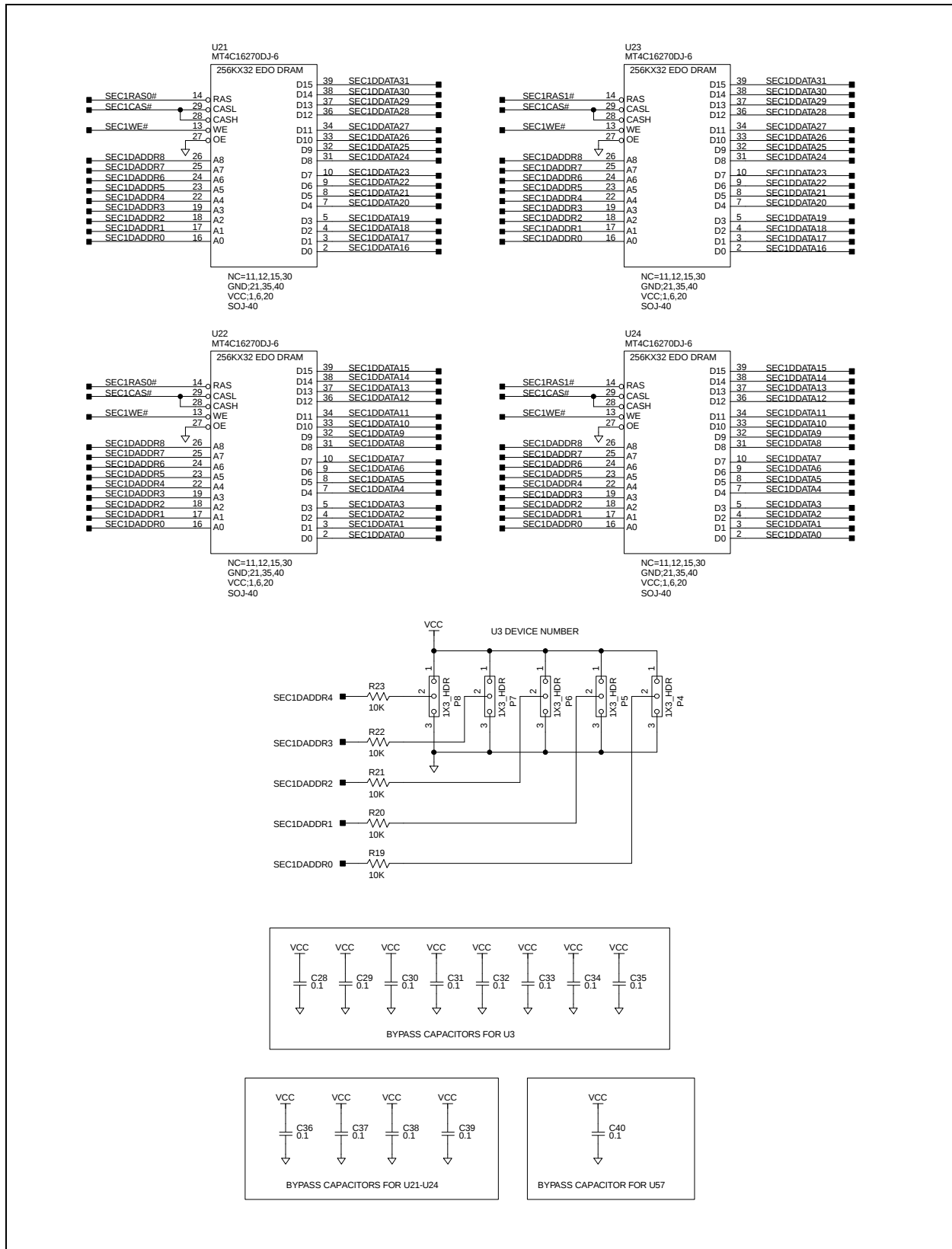
Switched Ethernet Reference Design—Sheet 3a



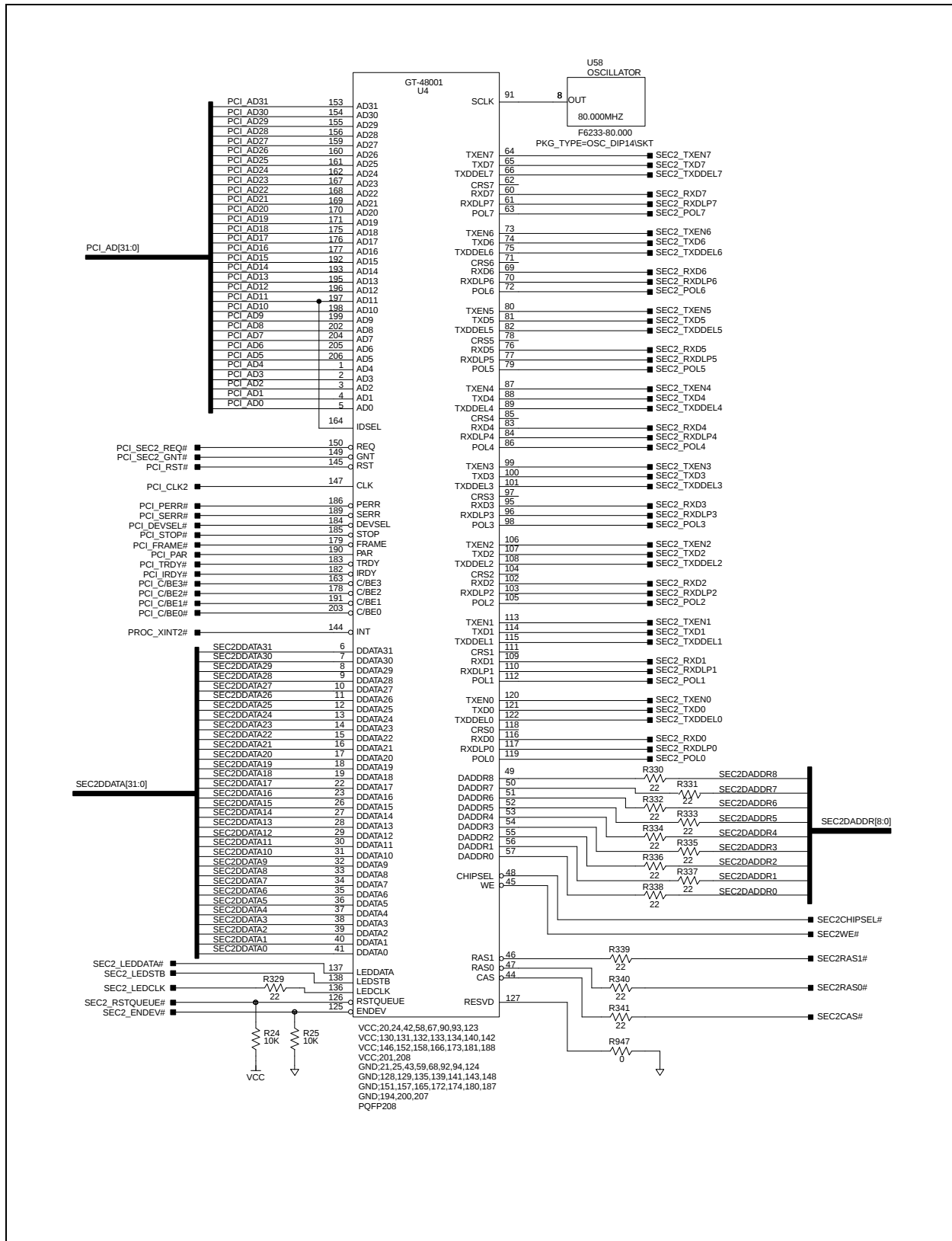
Switched Ethernet Reference Design—Sheet 3b



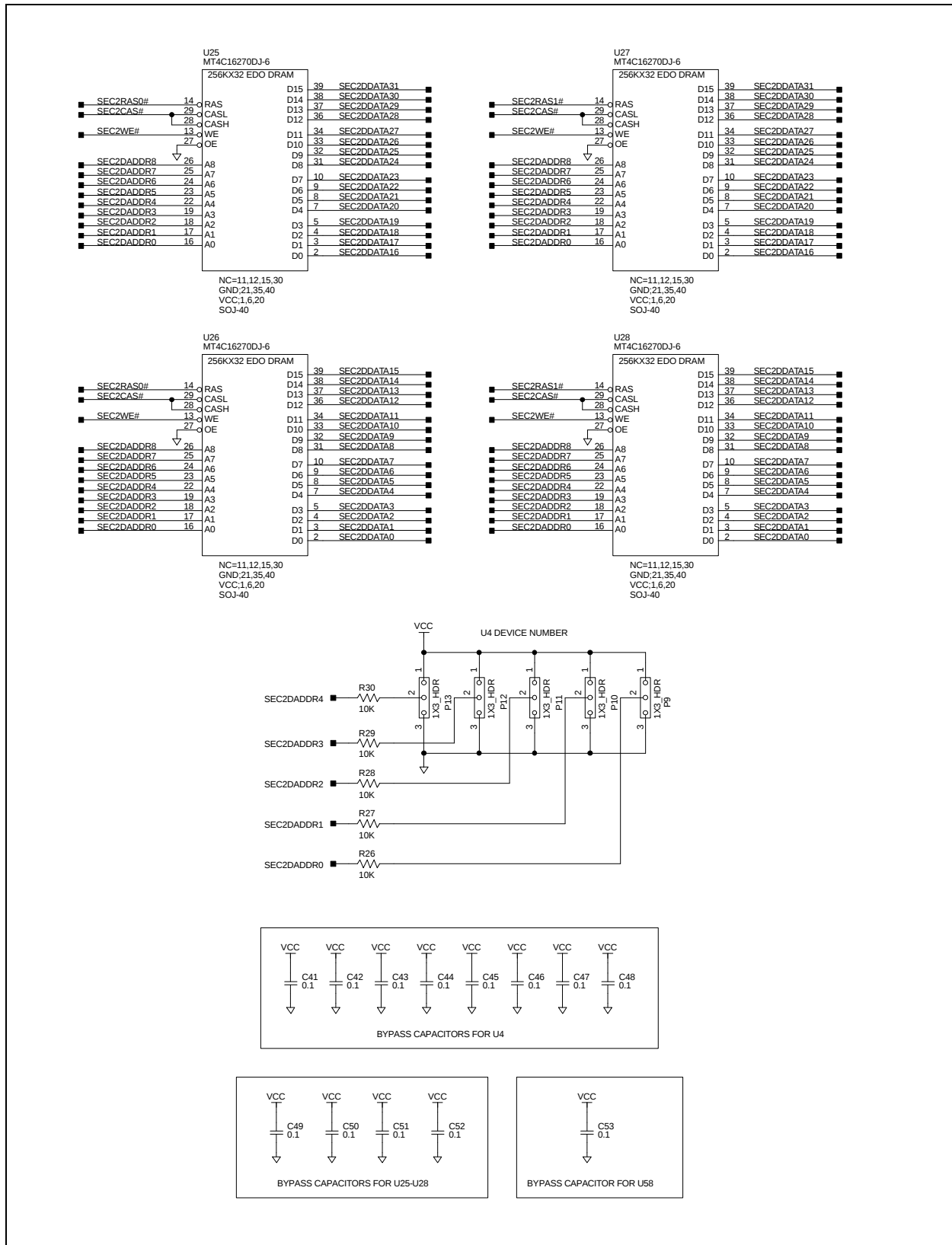
Switched Ethernet Reference Design—Sheet 4a



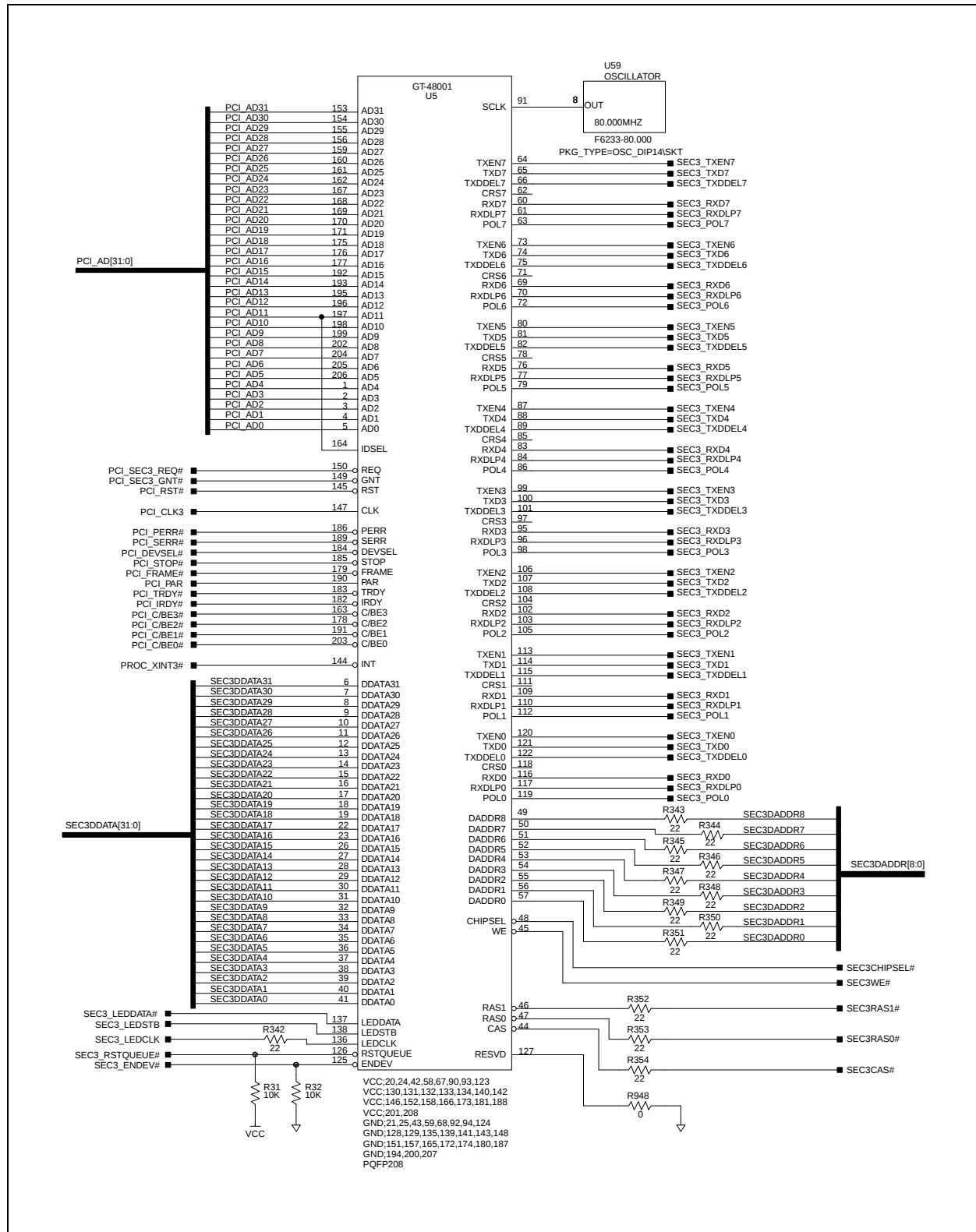
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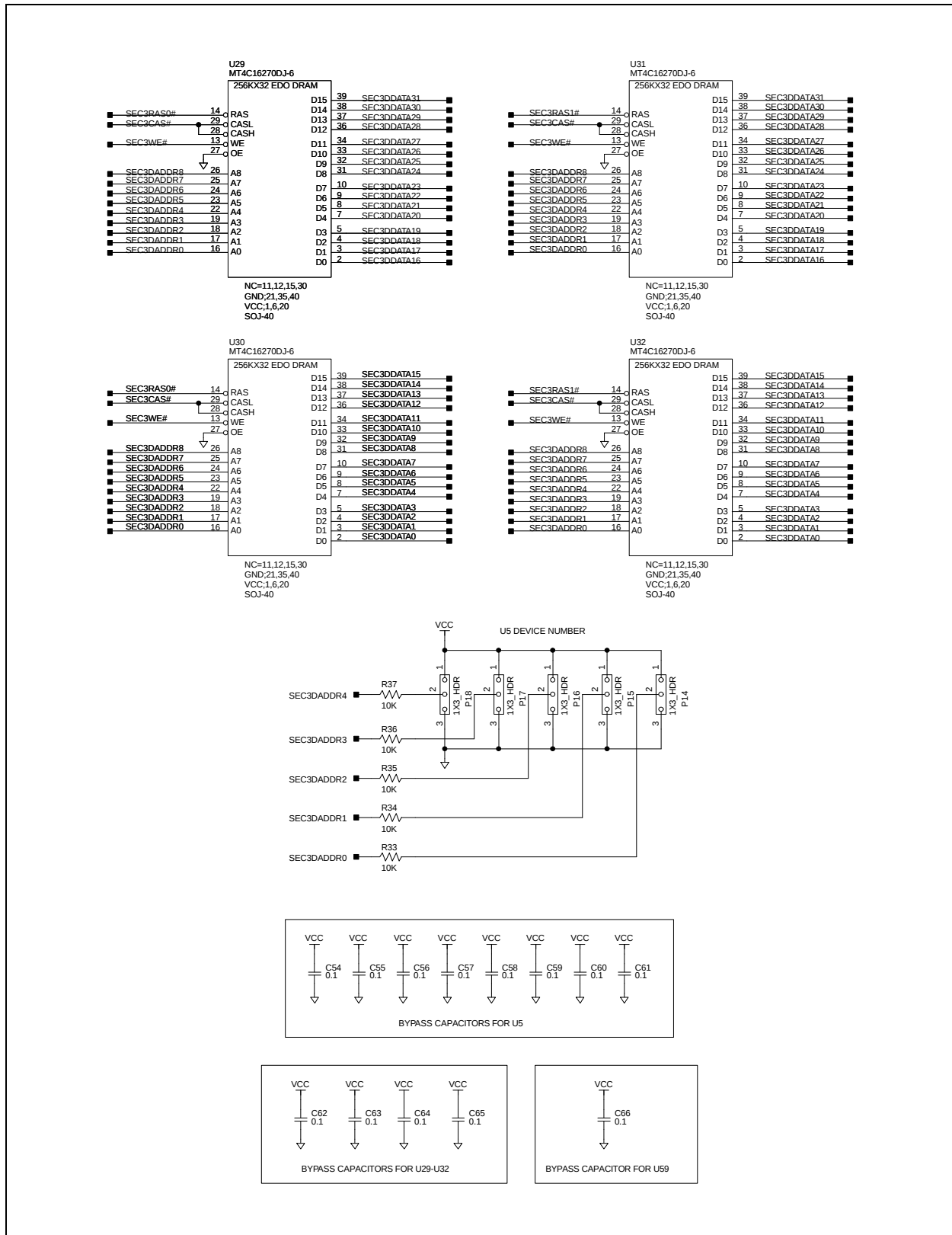
Switched Ethernet Reference Design—Sheet 5a



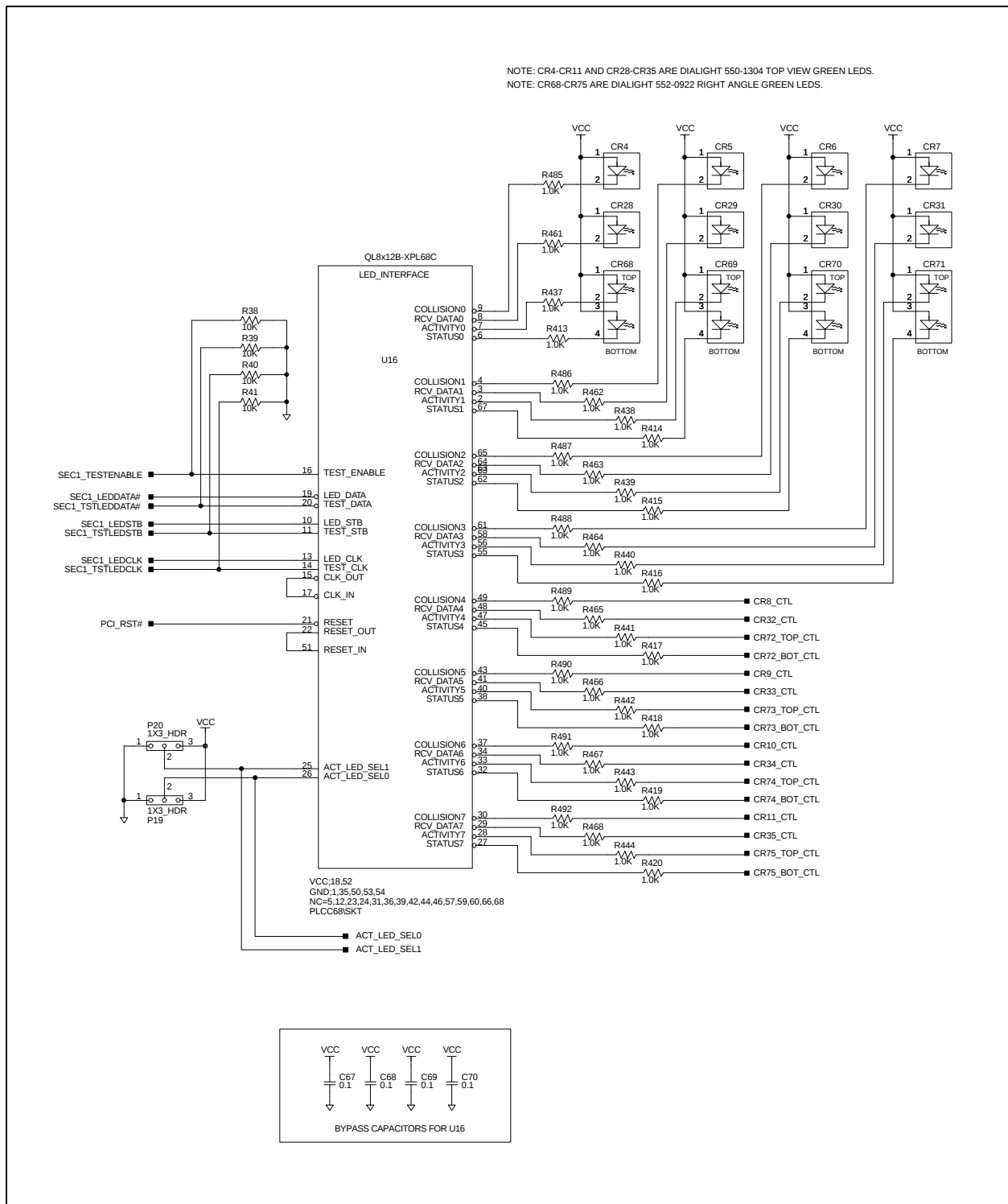
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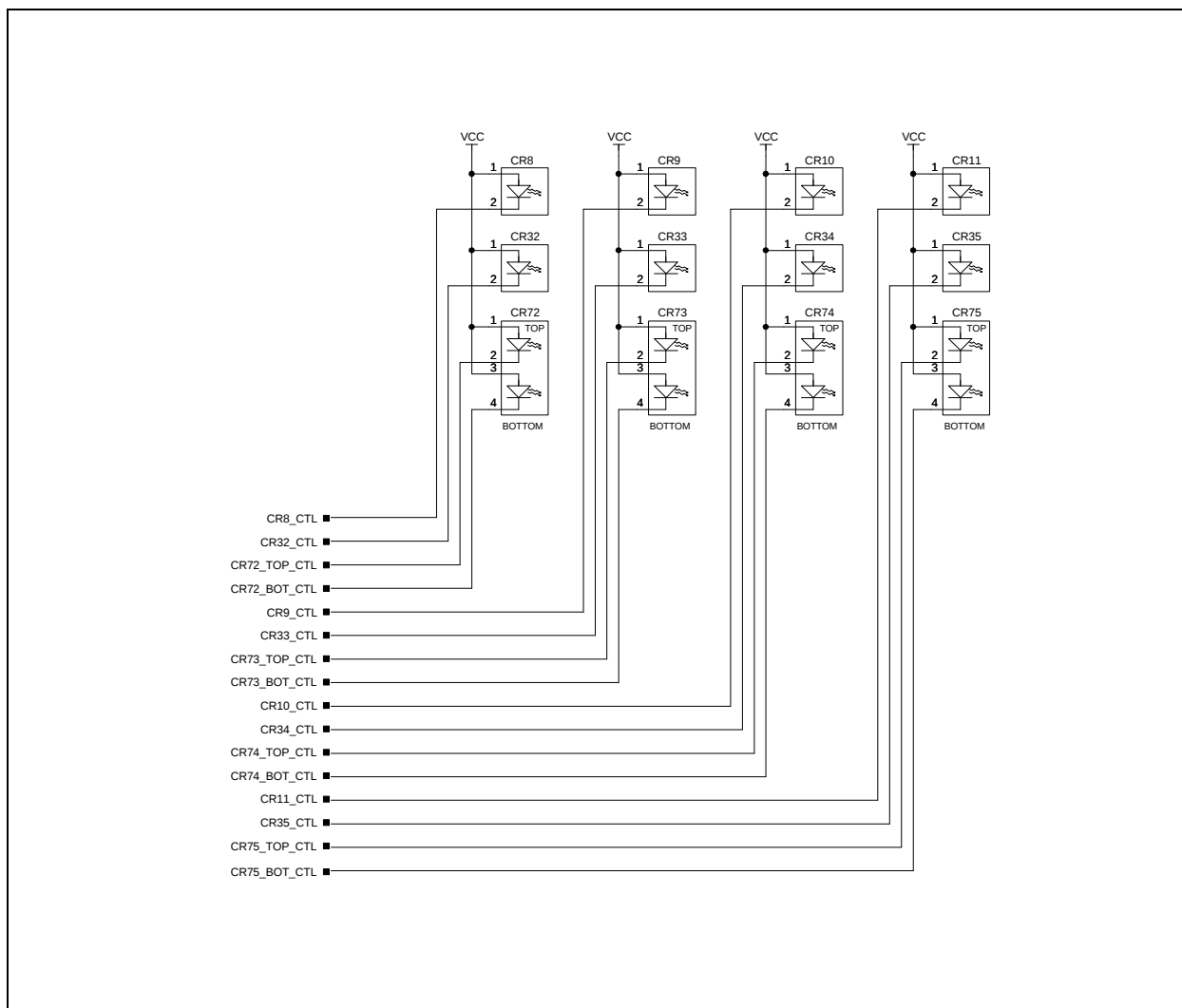
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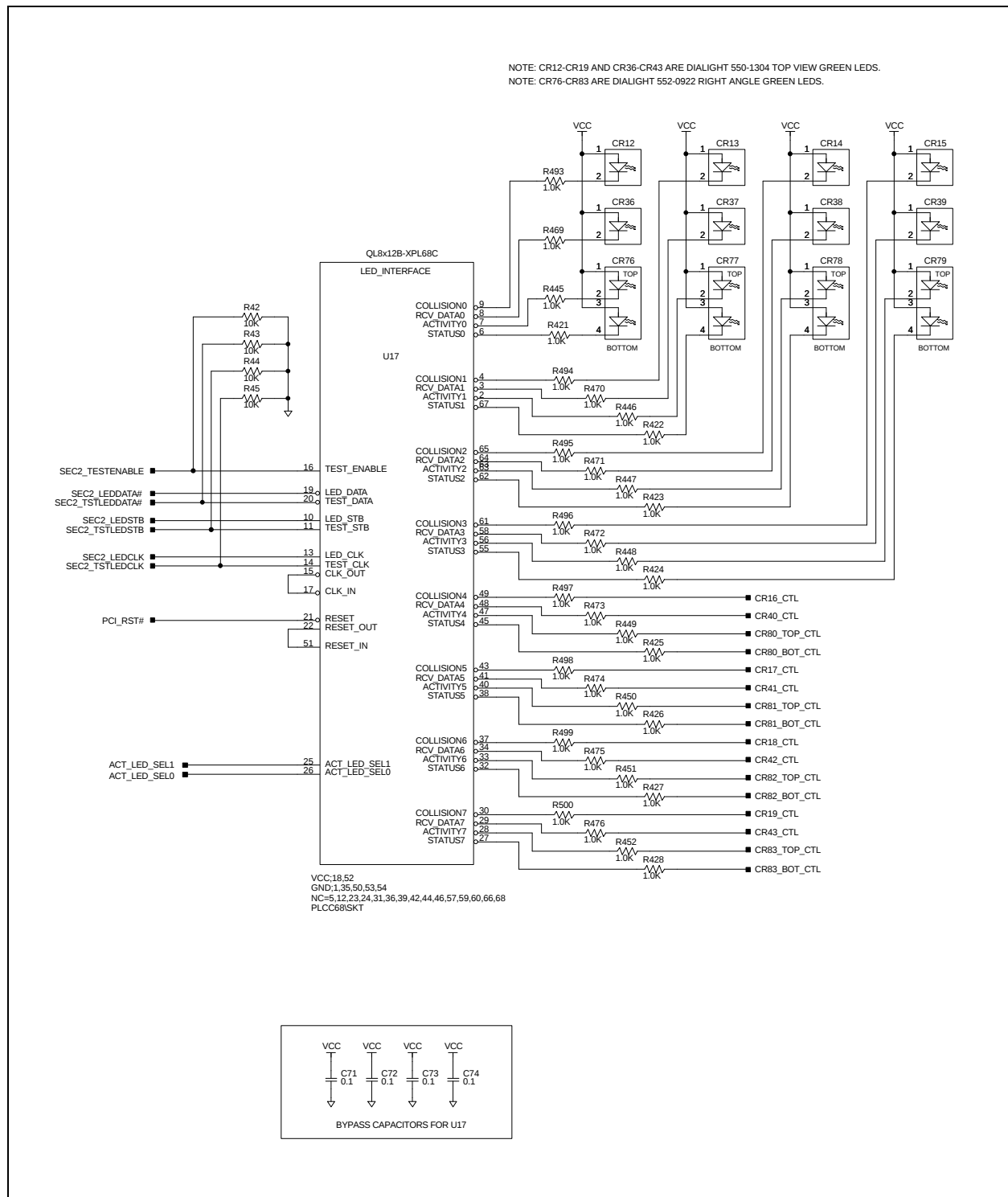
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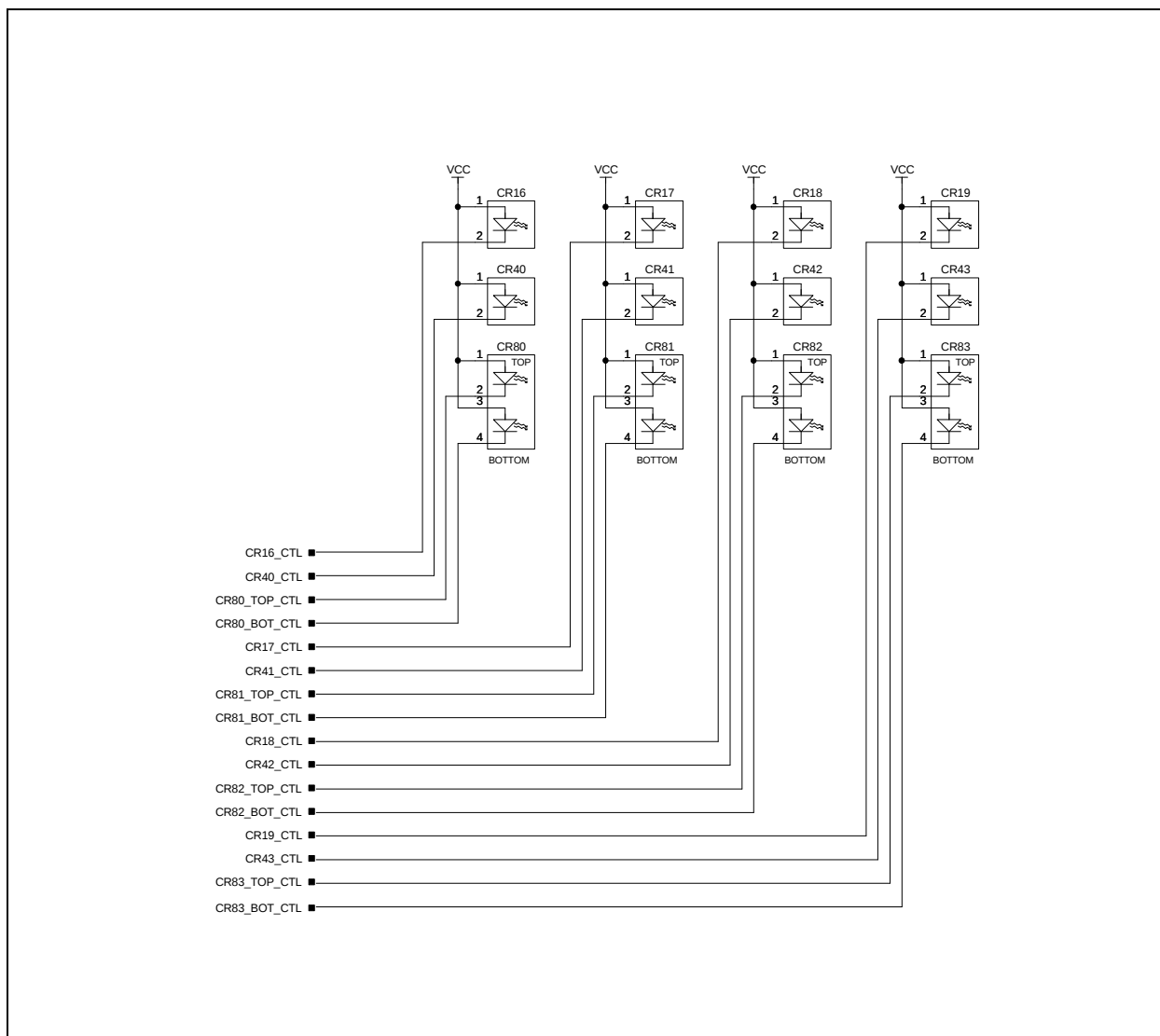
Switched Ethernet Reference Design—Sheet 7a



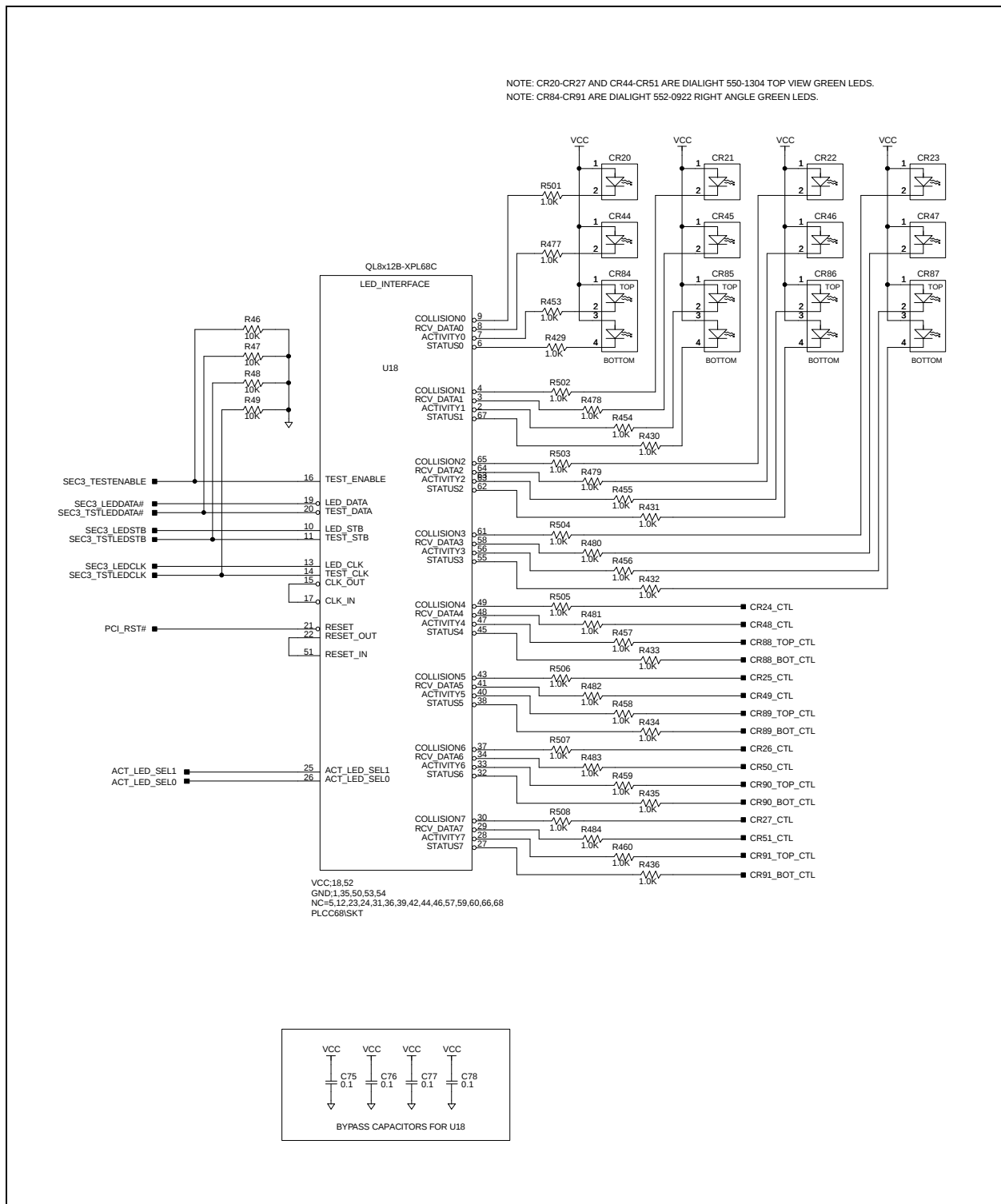
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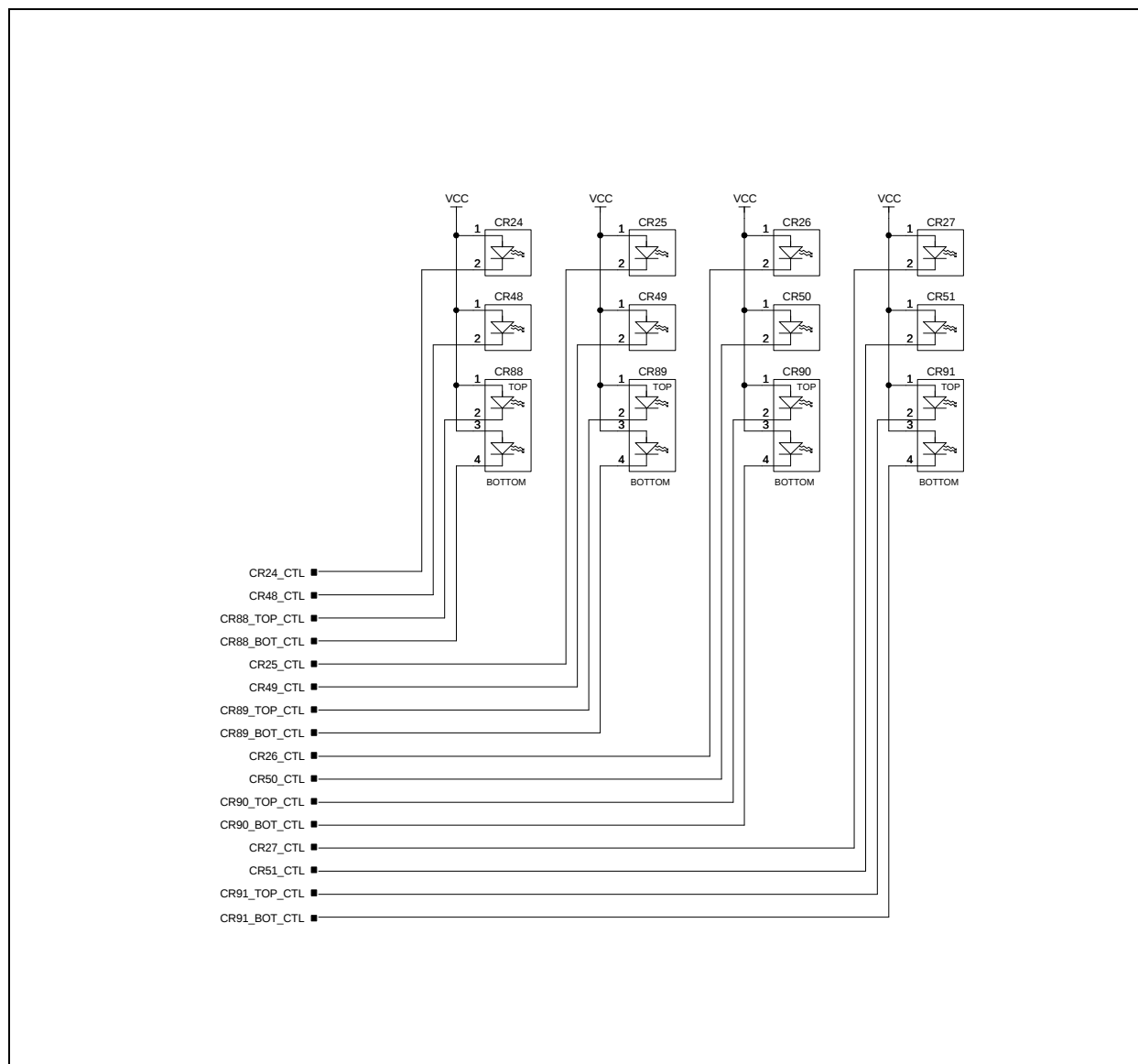
Switched Ethernet Reference Design—Sheet 8a



Switched Ethernet Reference Design—Sheet 8b



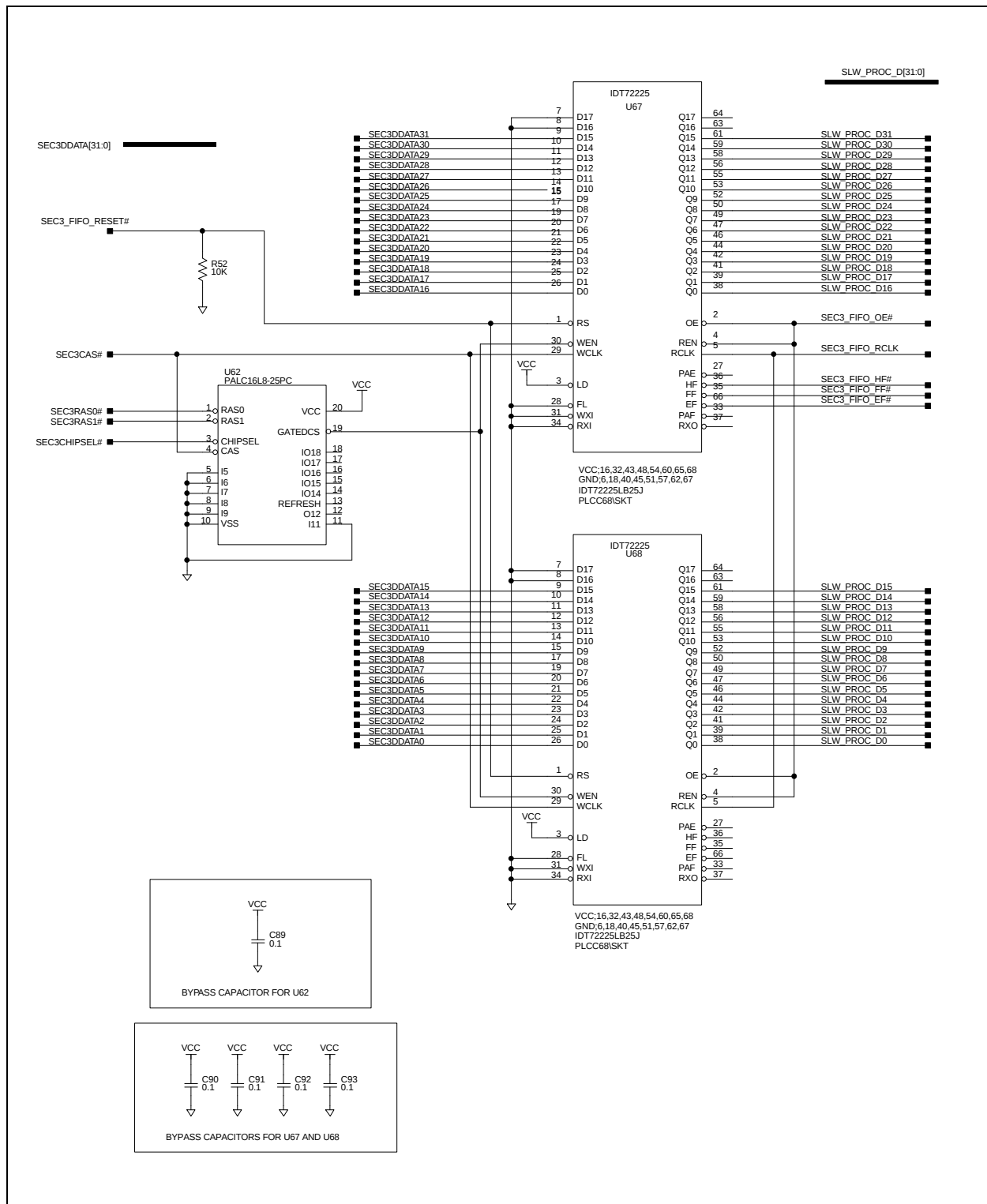
Switched Ethernet Reference Design—Sheet 9a



Switched Ethernet Reference Design—Sheet 9b



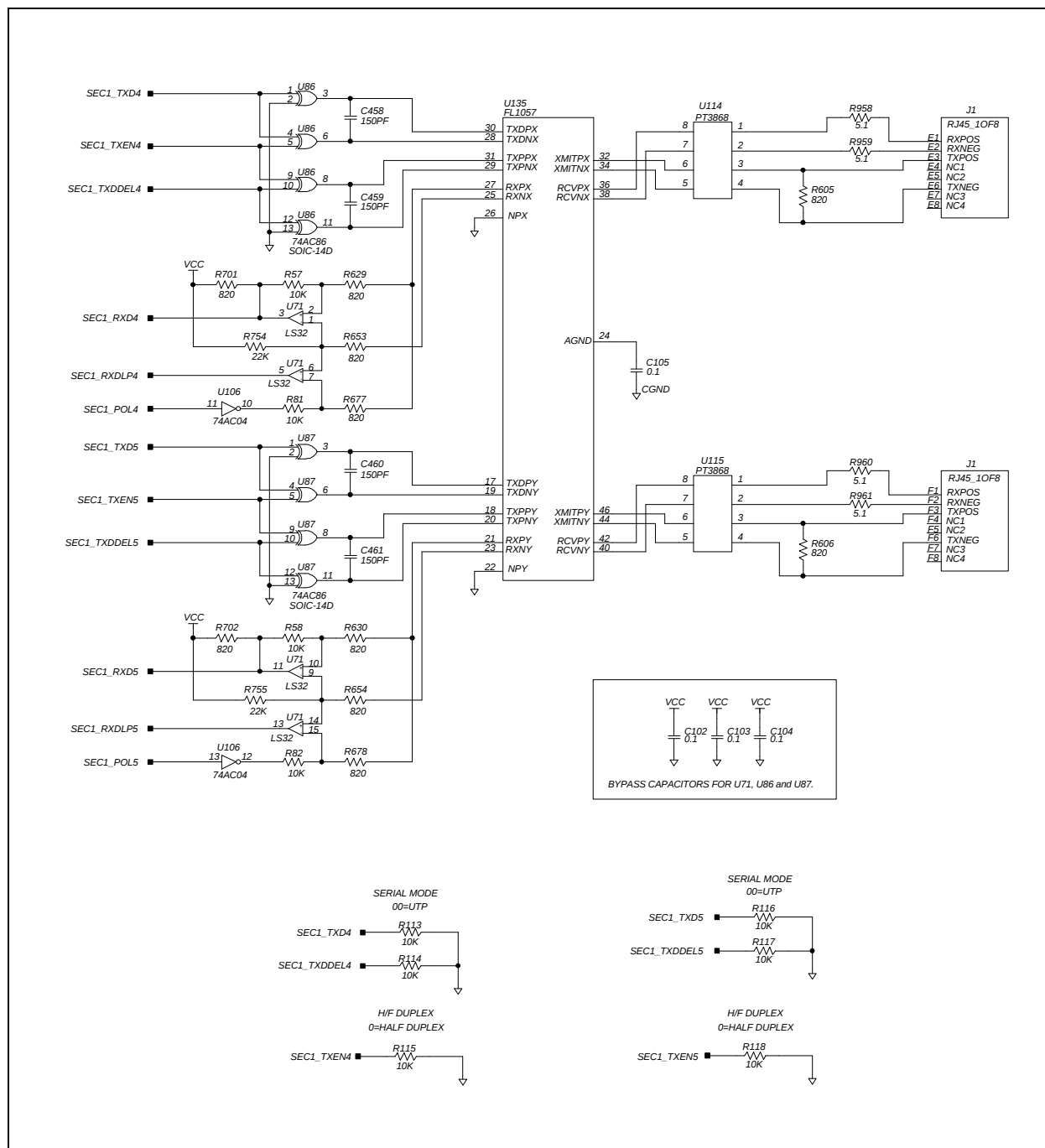




Switched Ethernet Reference Design—Sheet 12





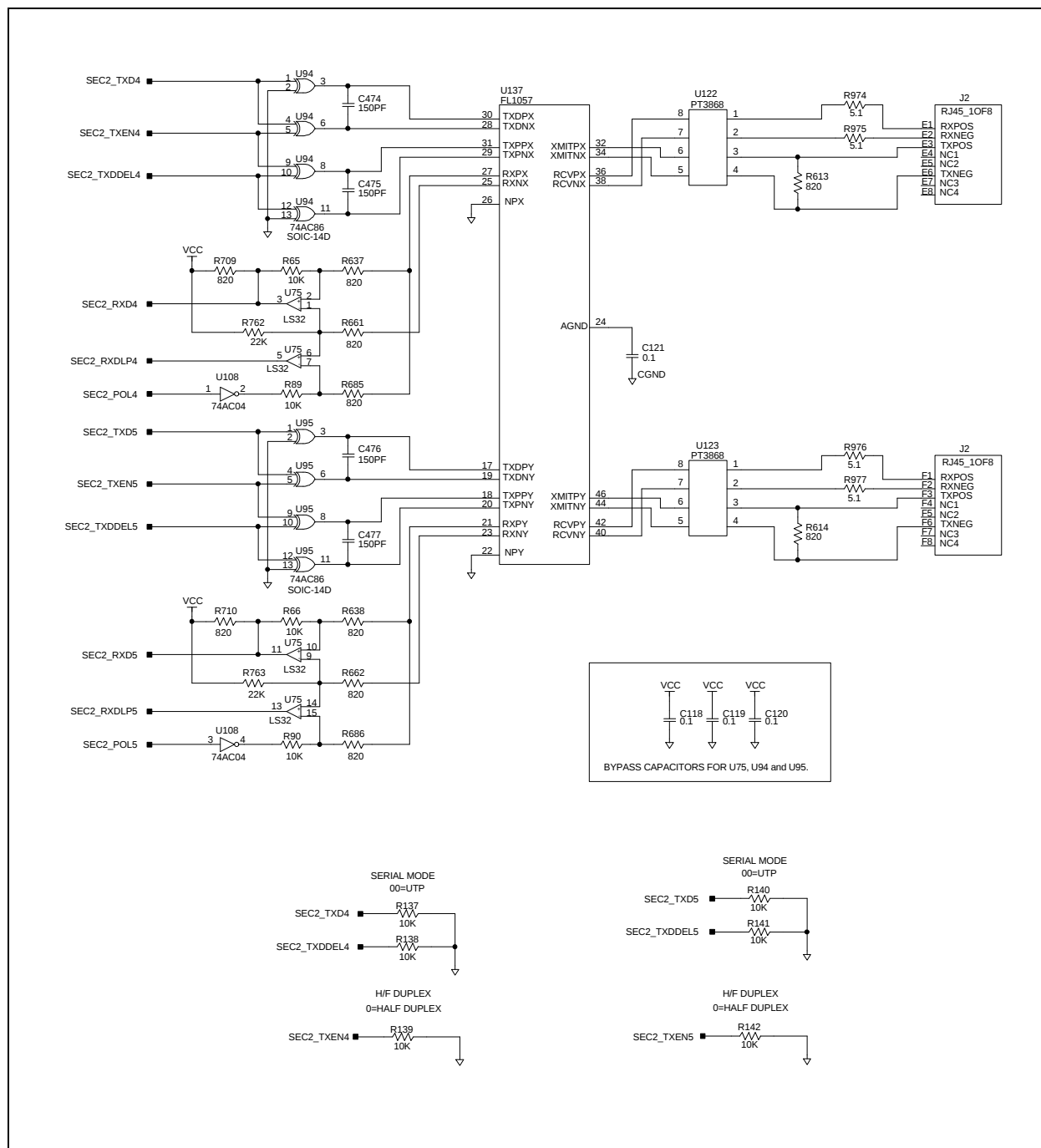


Switched Ethernet Reference Design—Sheet 15





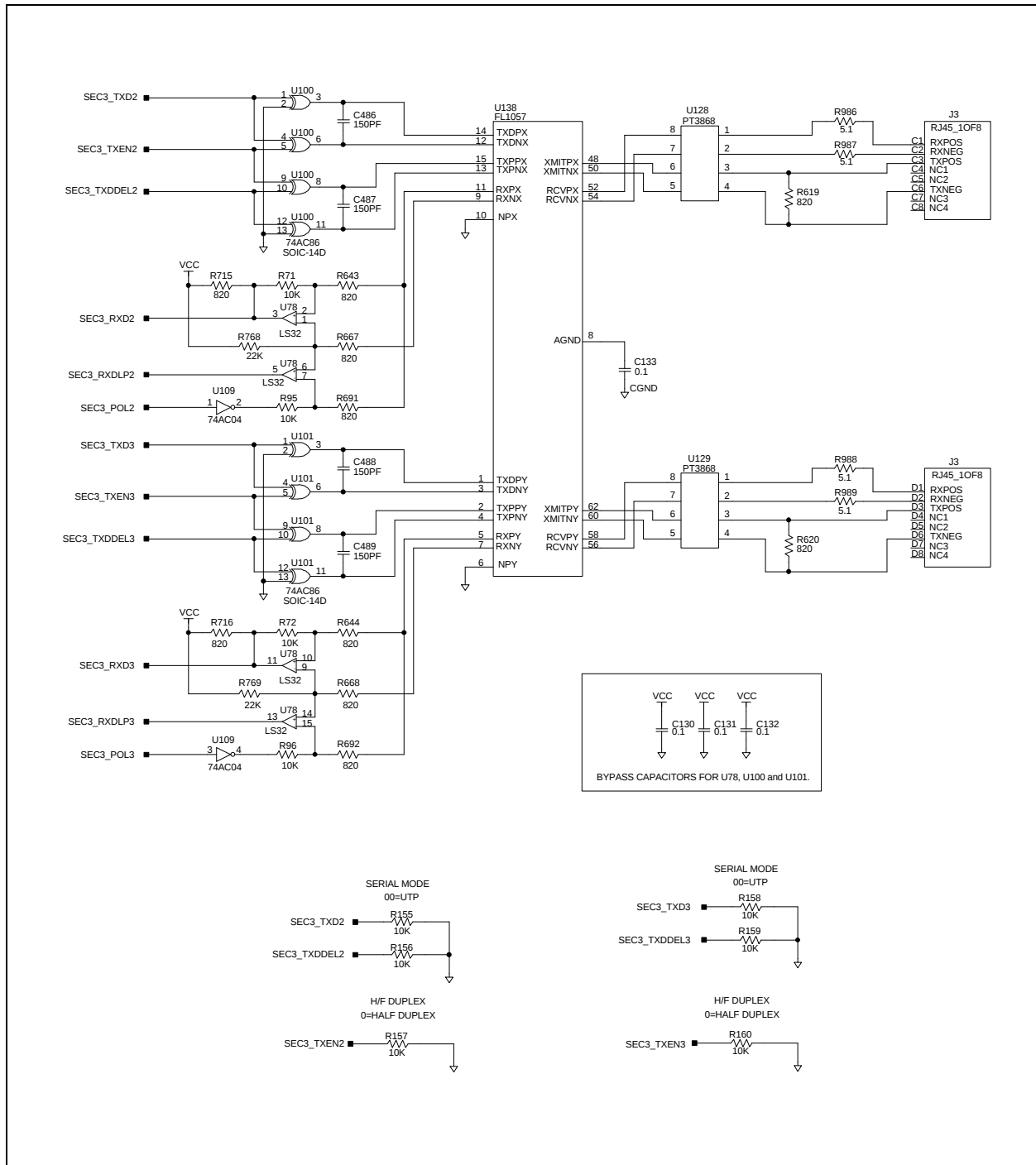




Switched Ethernet Reference Design—Sheet 19

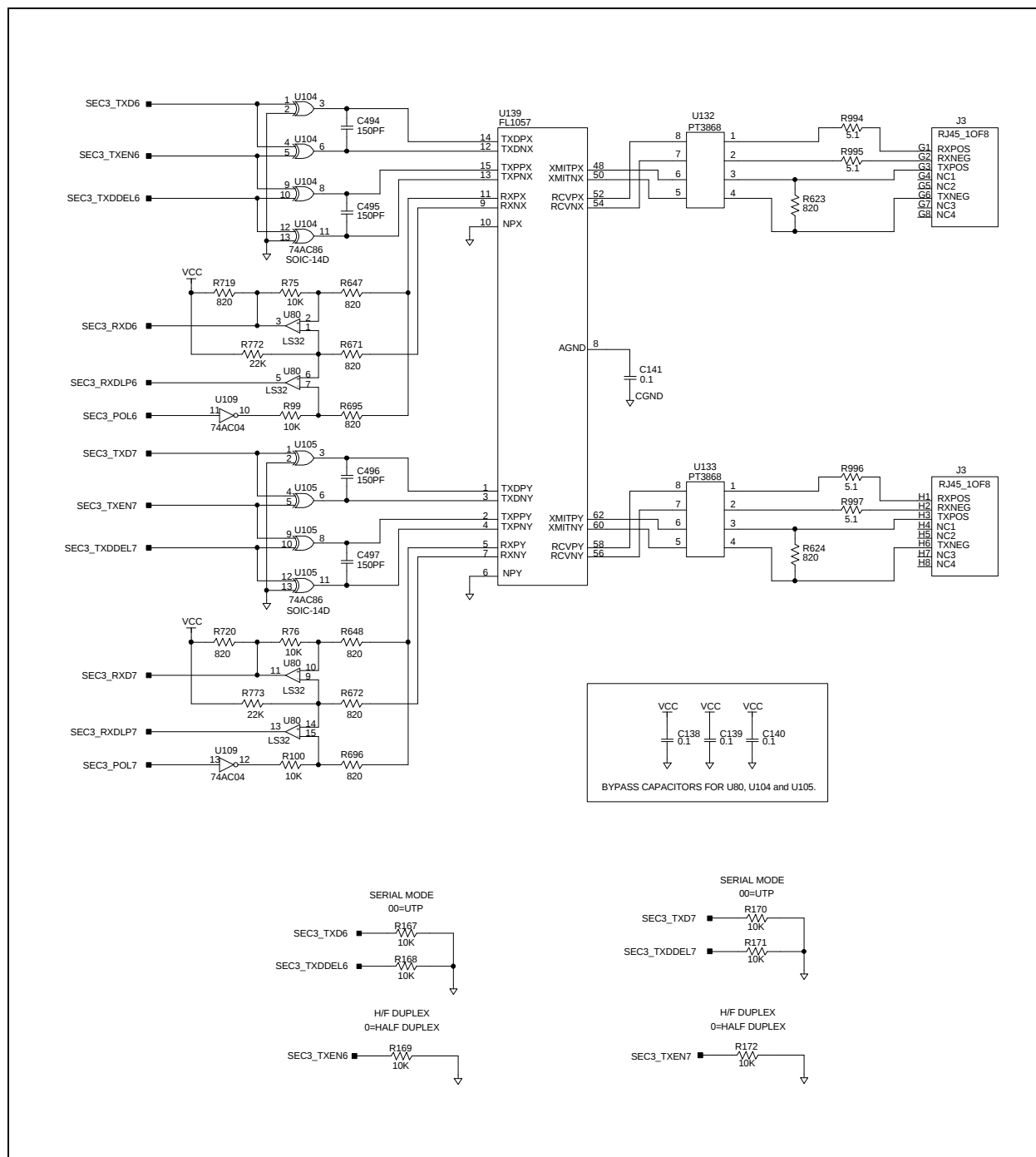




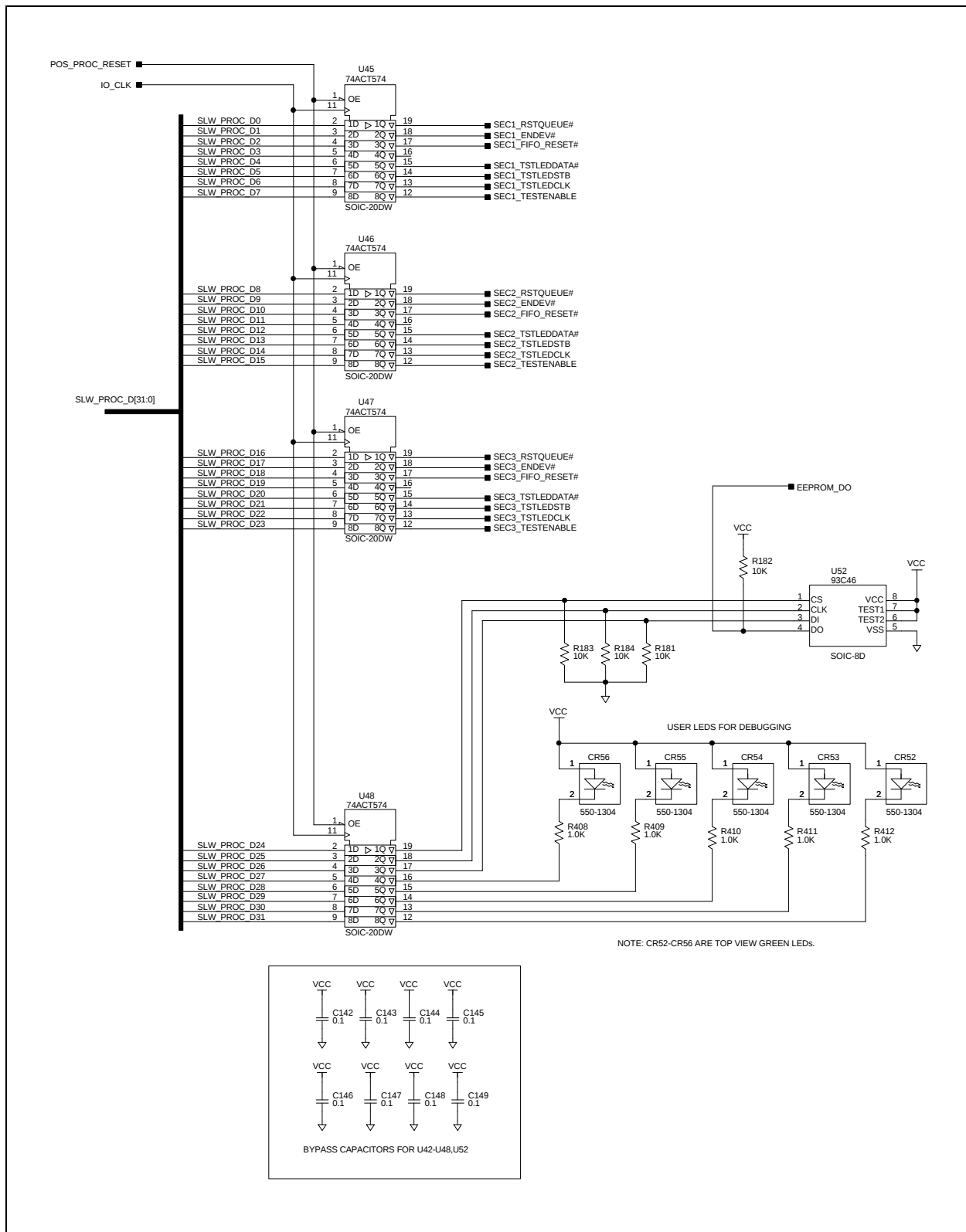


Switched Ethernet Reference Design—Sheet 22

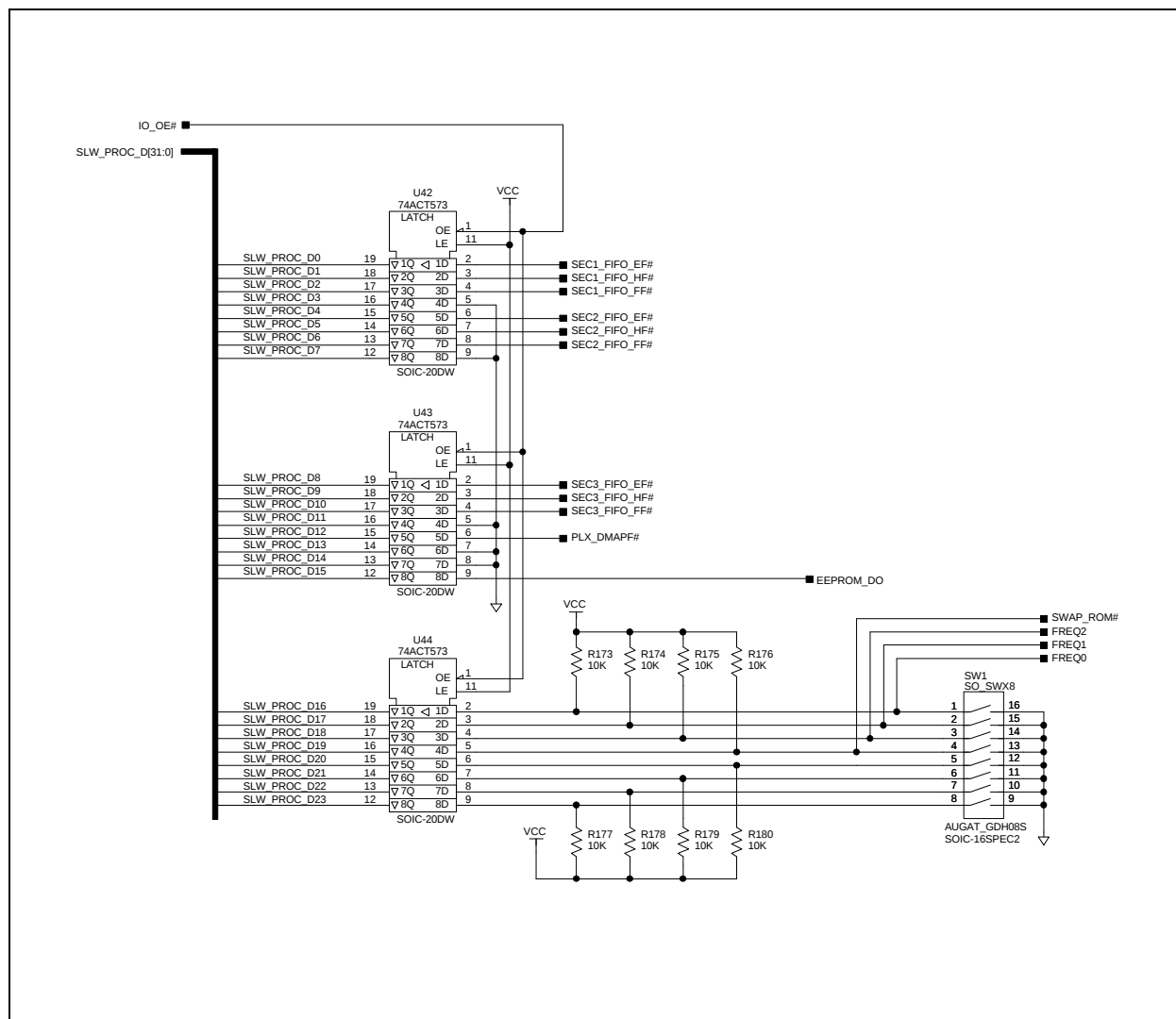




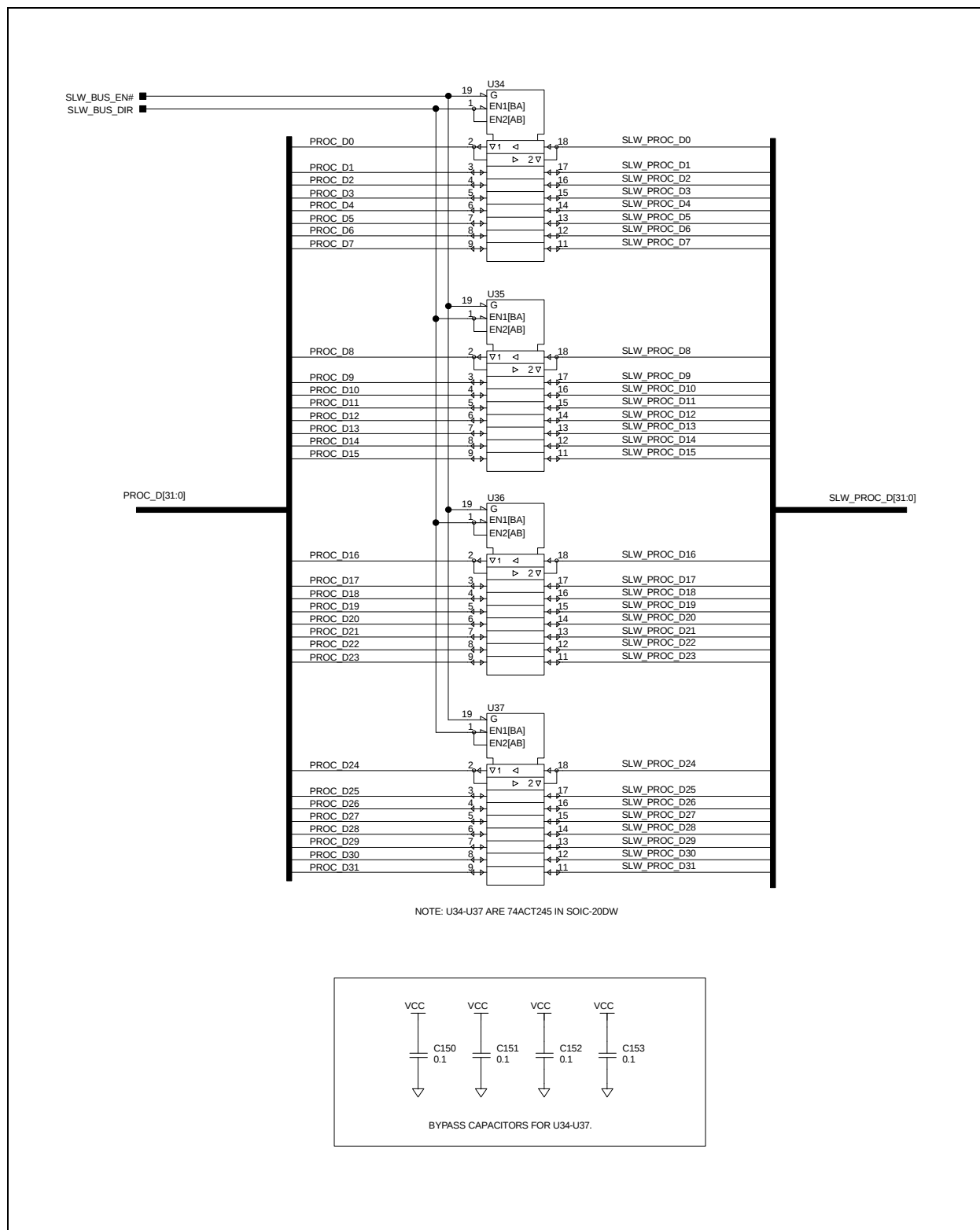
Switched Ethernet Reference Design—Sheet 24



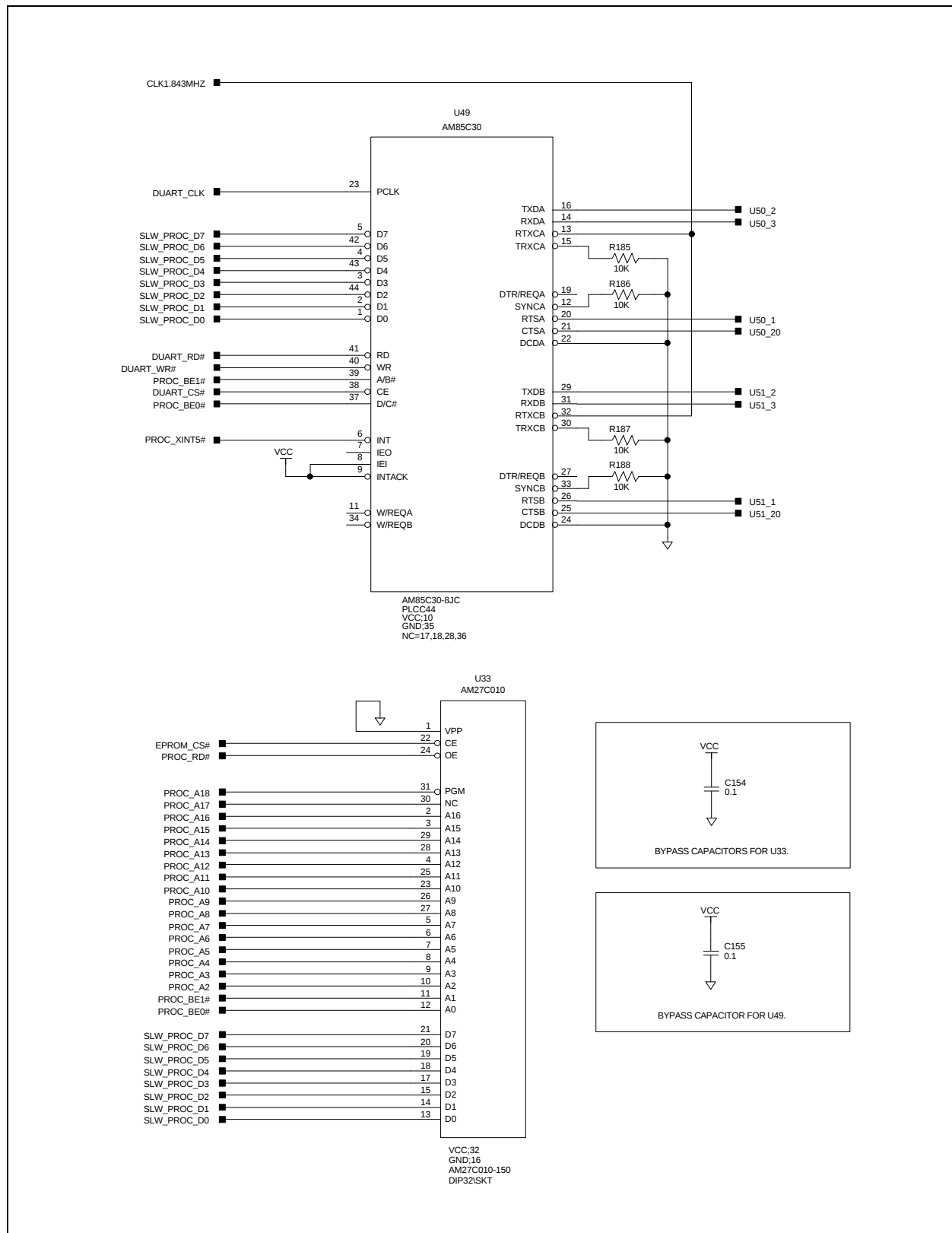
Switched Ethernet Reference Design—Sheet 25a



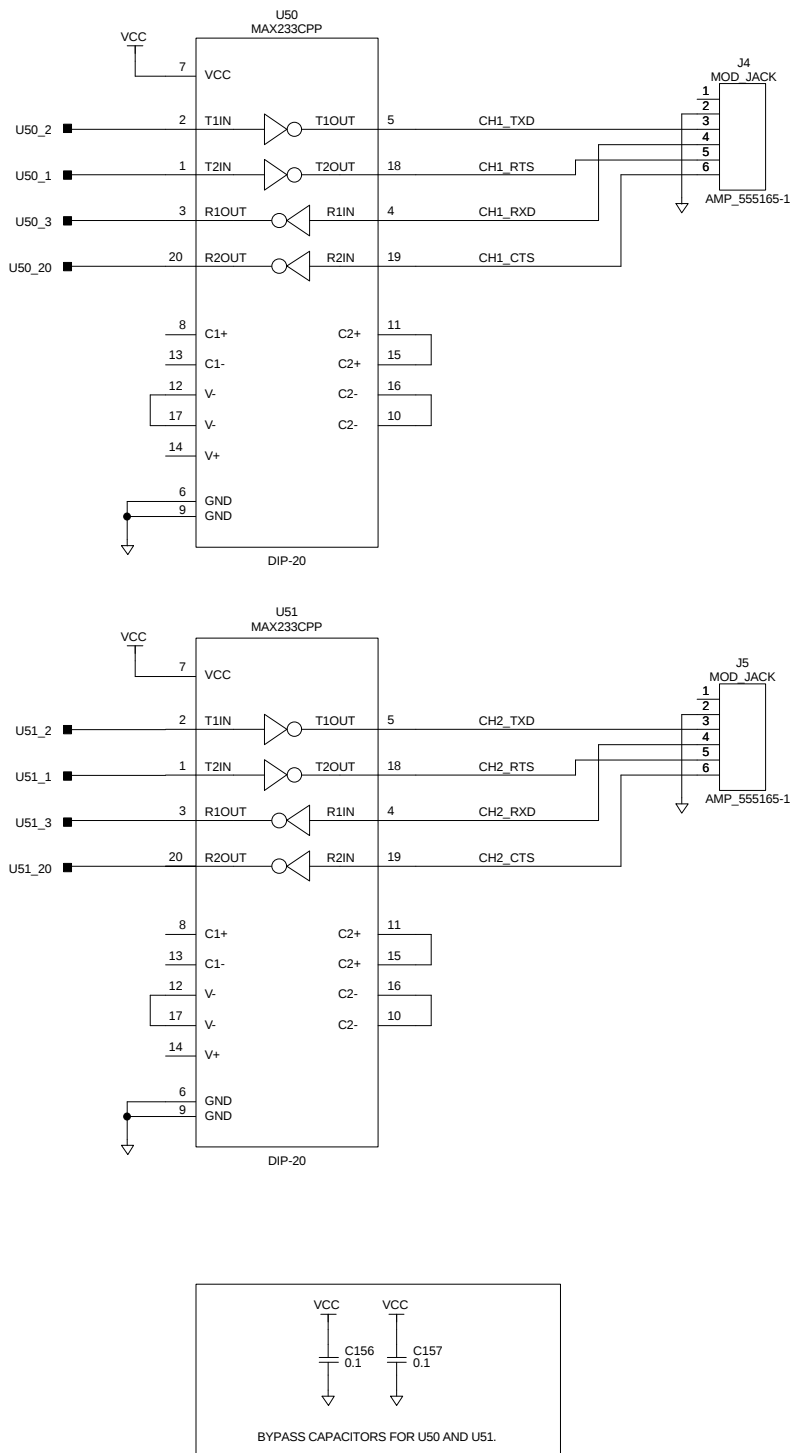
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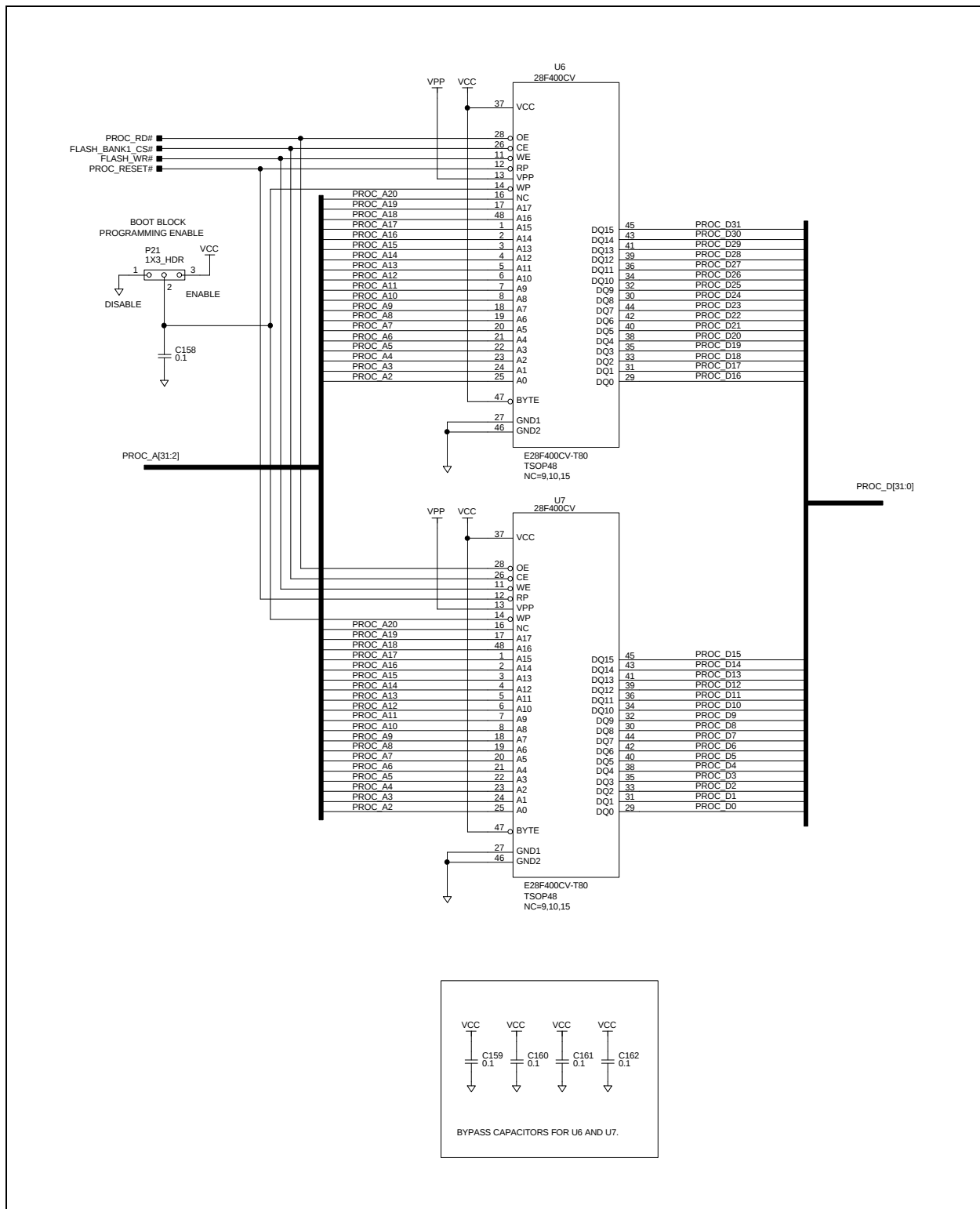
Switched Ethernet Reference Design—Sheet 26



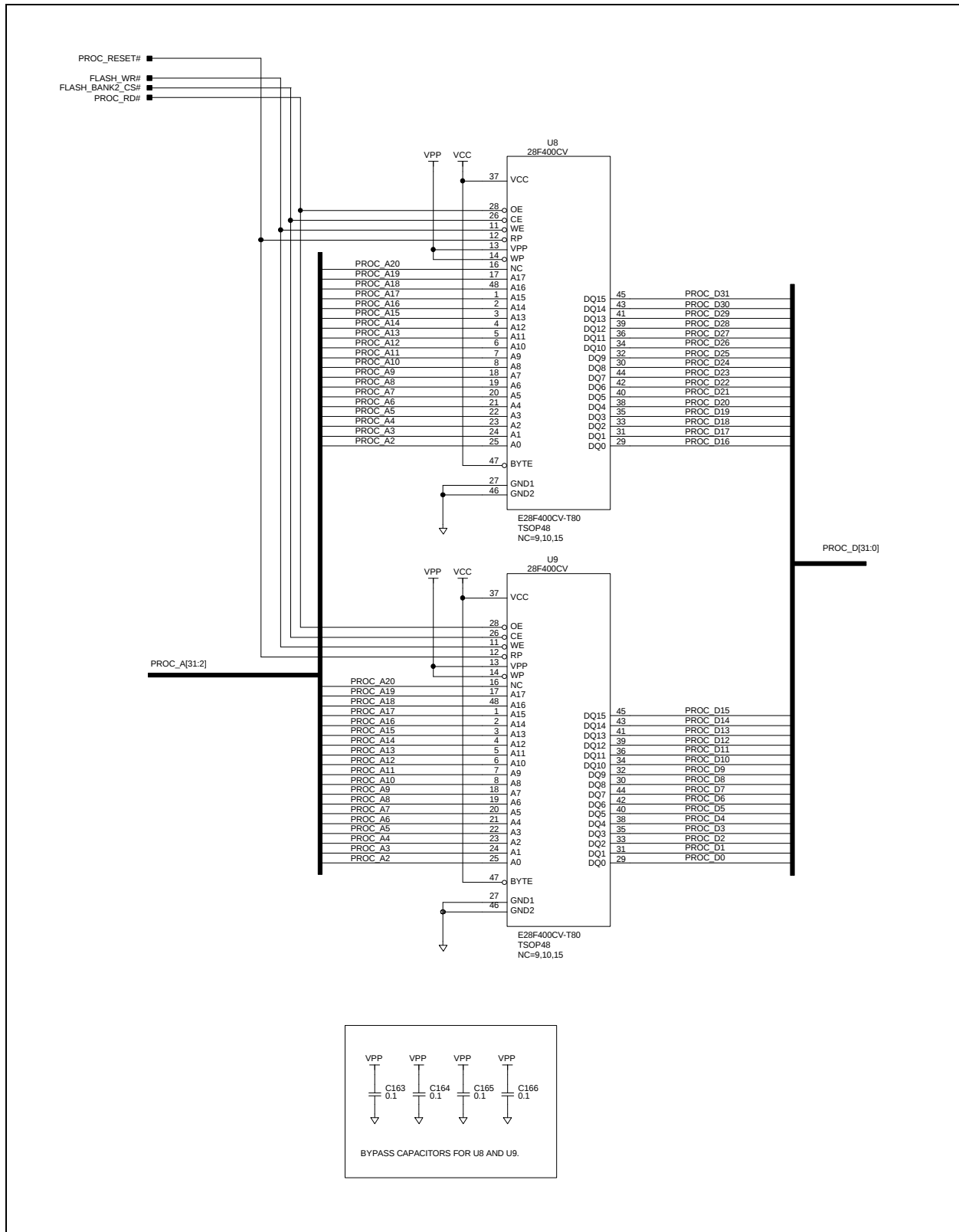
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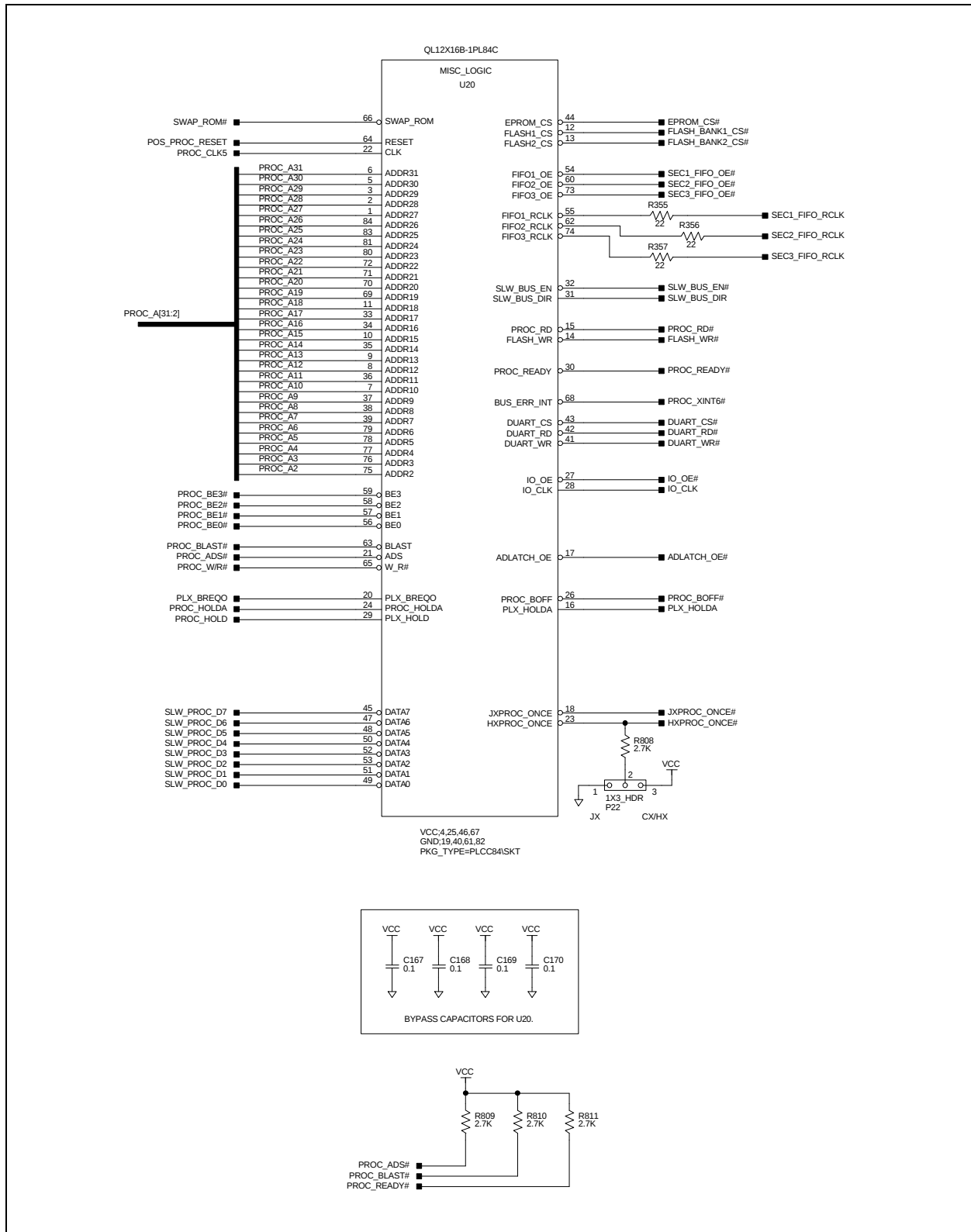
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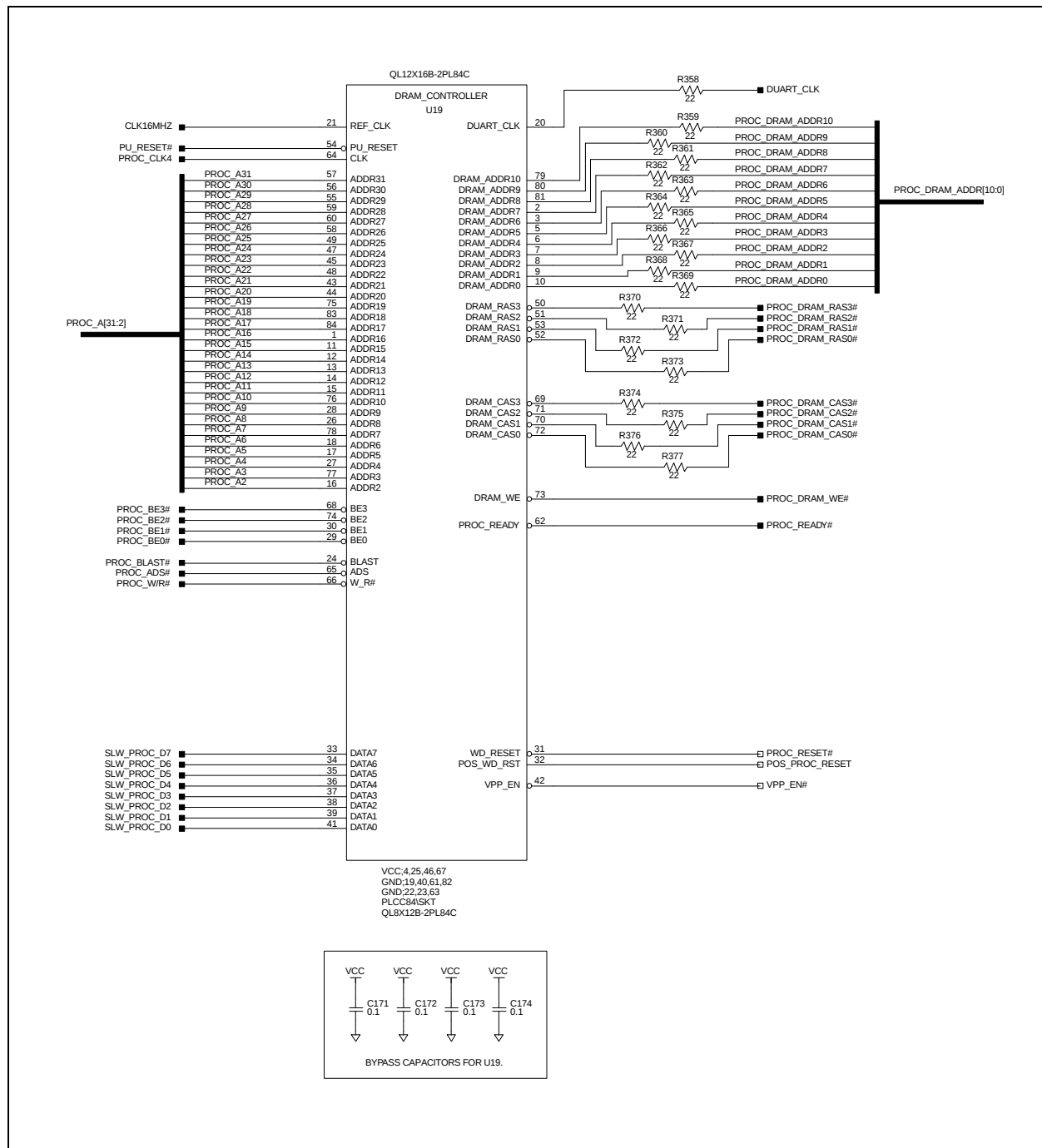
Switched Ethernet Reference Design—Sheet 28a



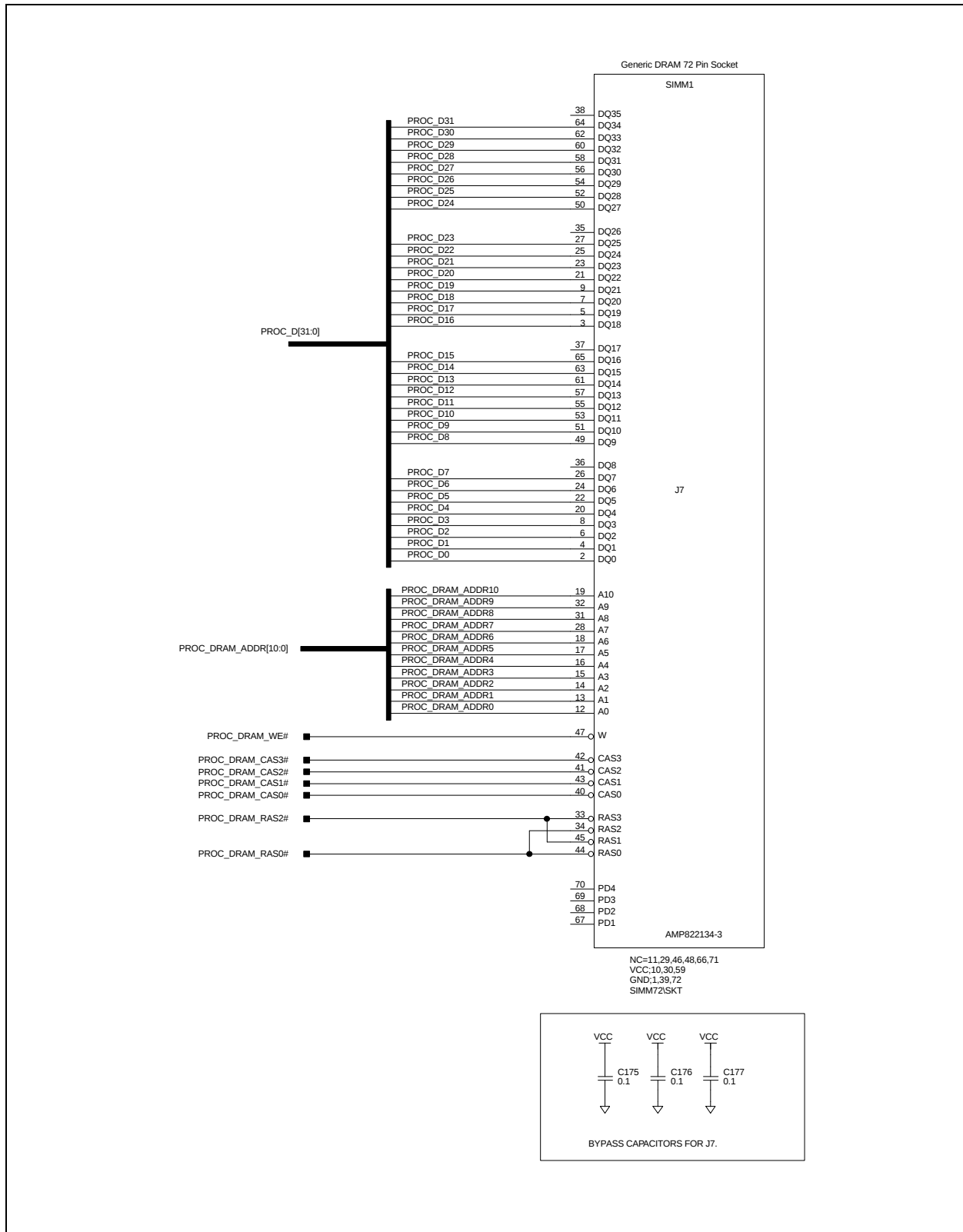
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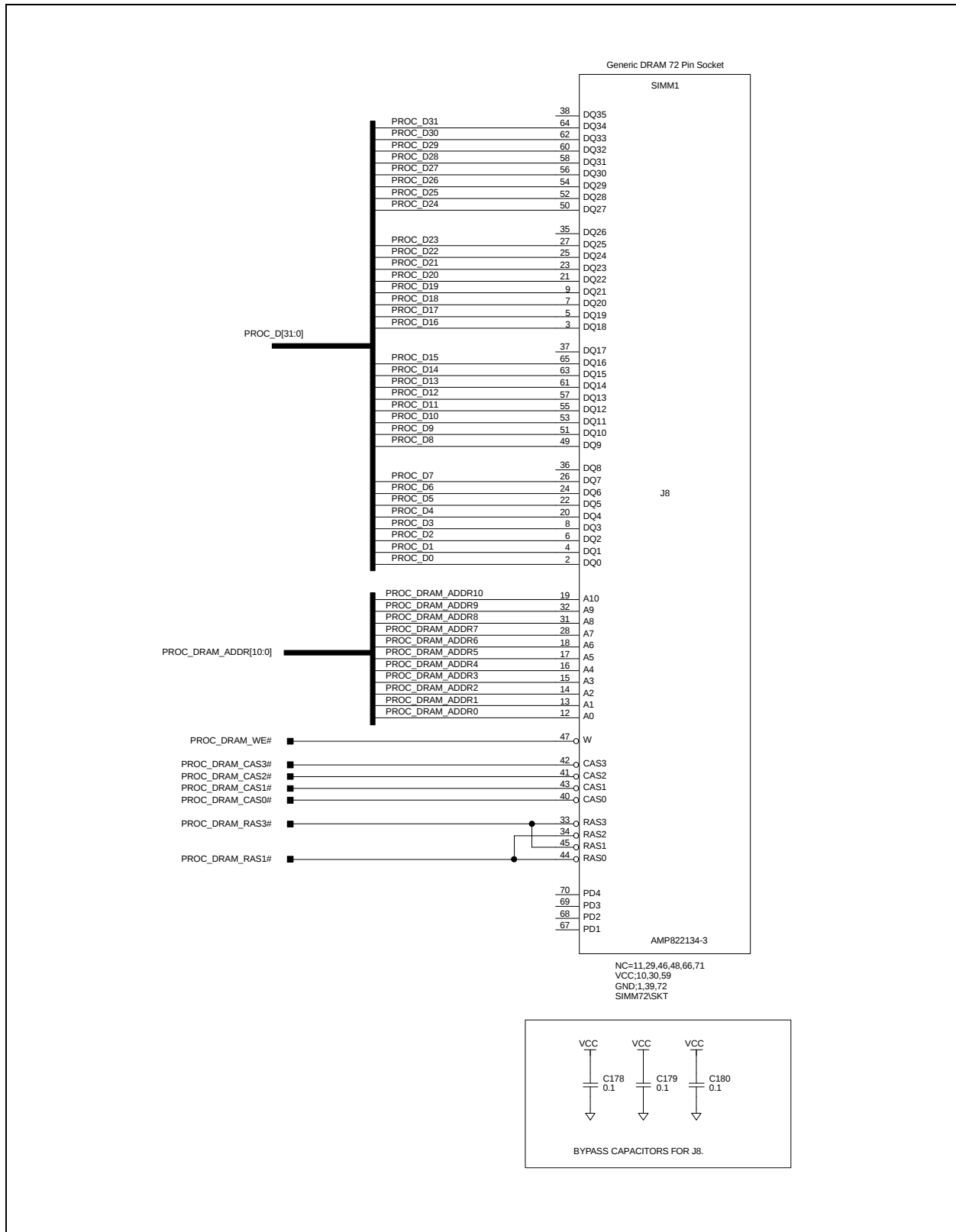
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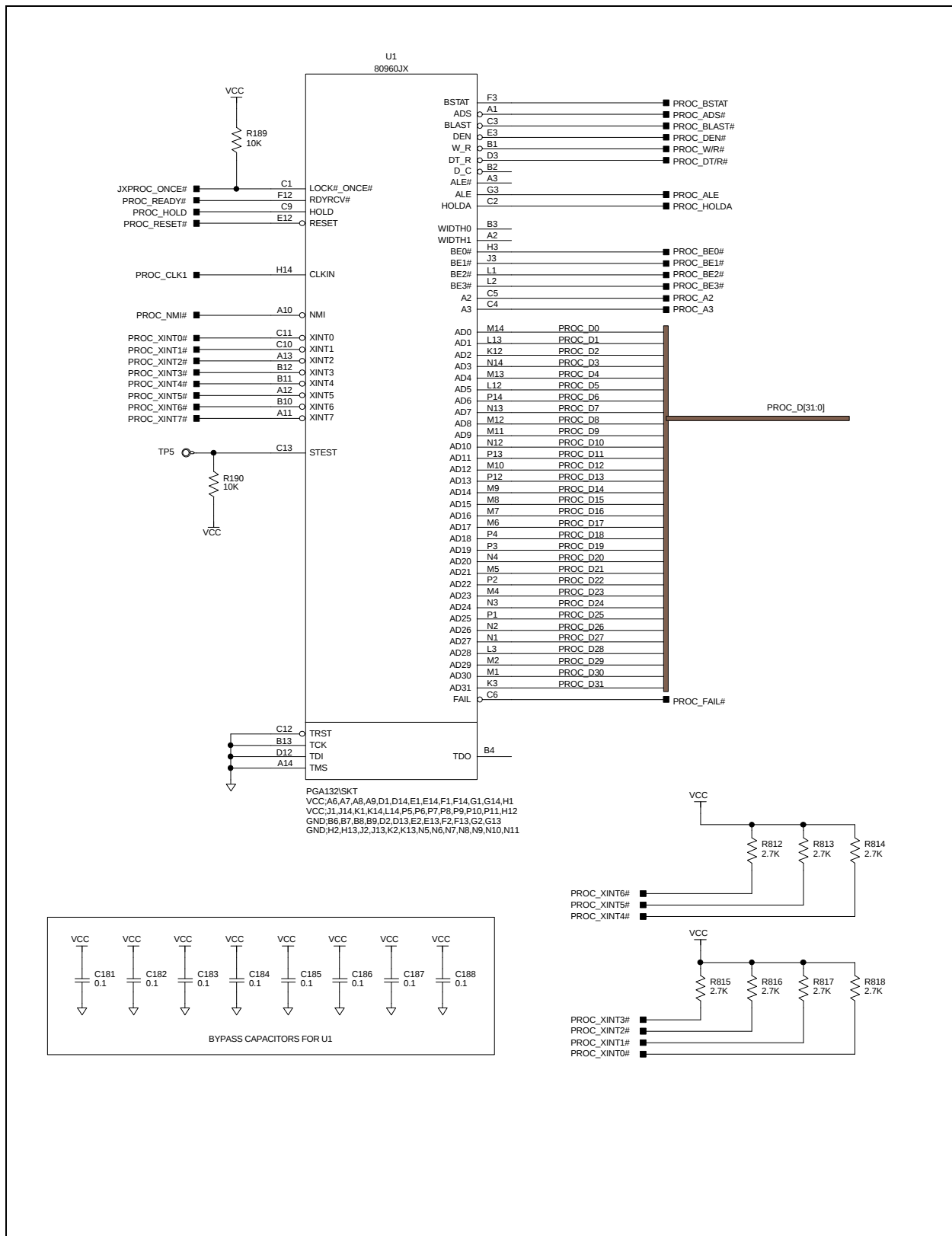
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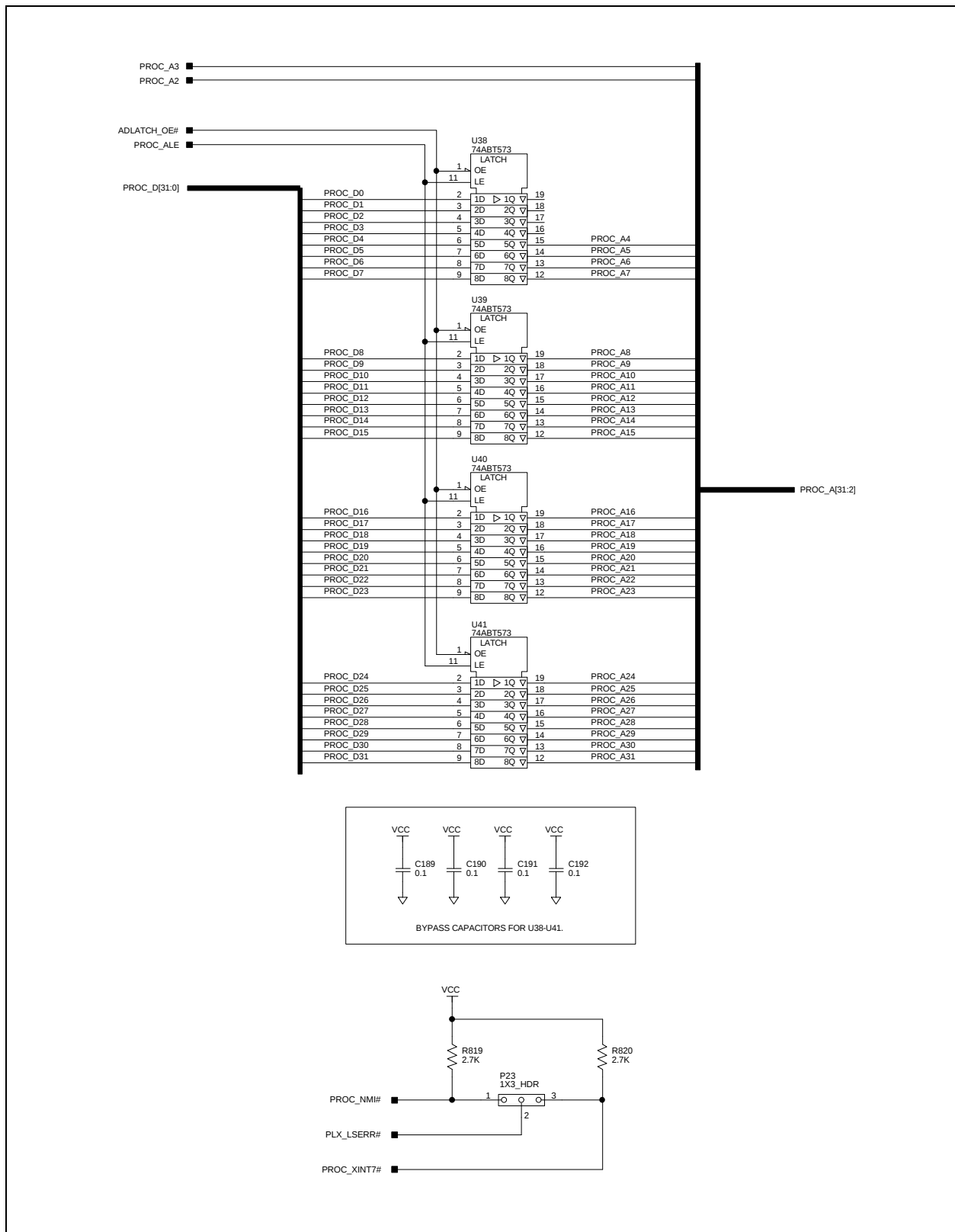
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Switched Ethernet Reference Design—Sheet 30b

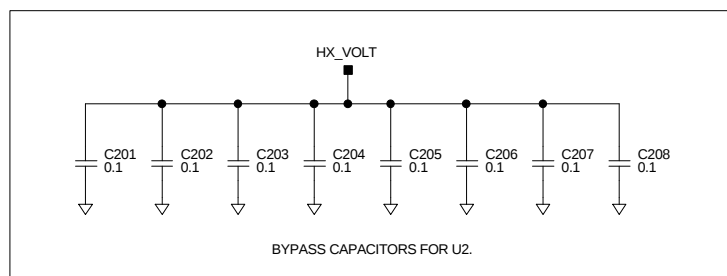
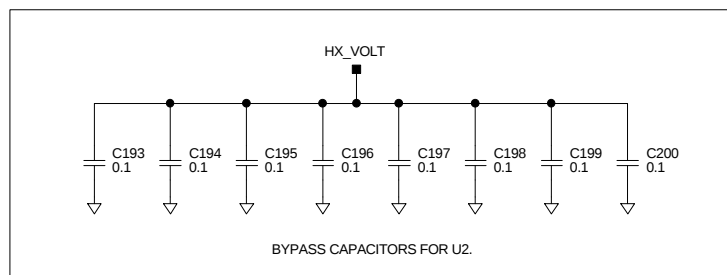
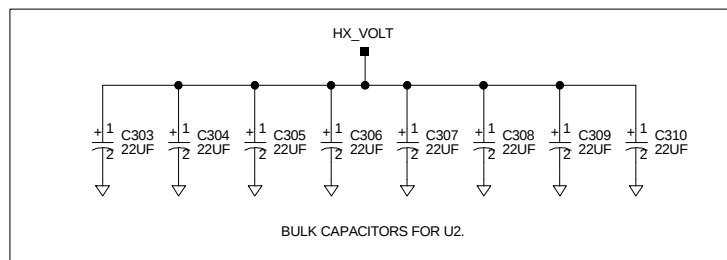
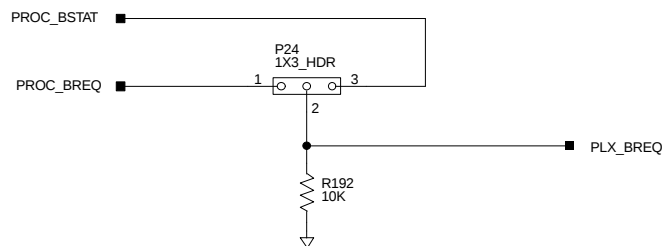


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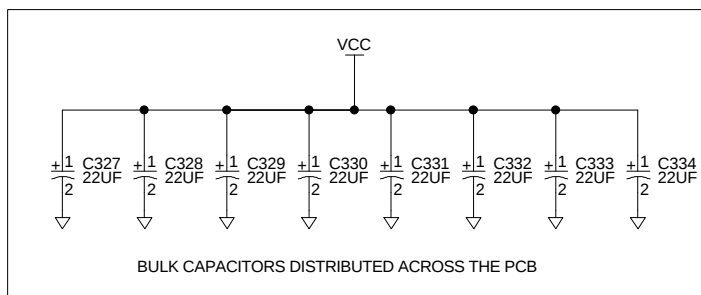
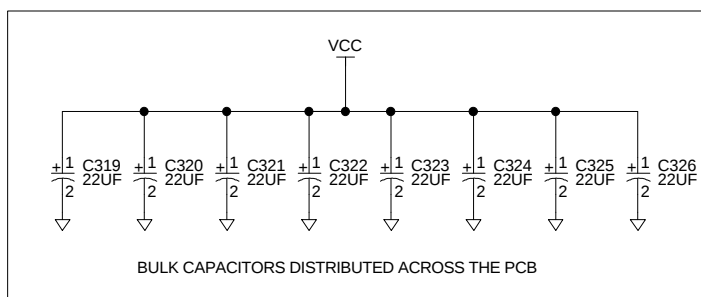
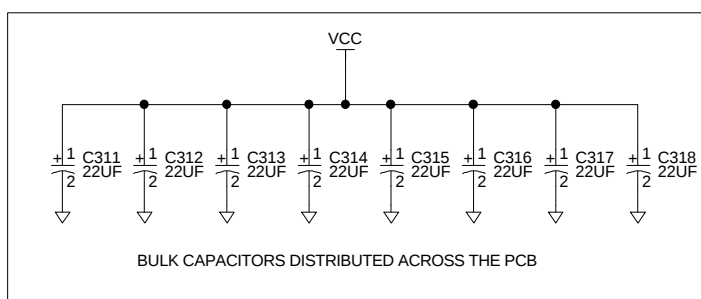
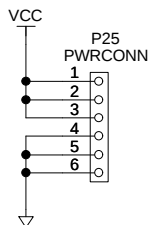
Switched Ethernet Reference Design—Sheet 31b





Switched Ethernet Reference Design—Sheet 32b





Switched Ethernet Reference Design—Sheet 33b