# Structured ASIC

**From the Paper,**
**"Paradigm shift in ASIC technology**
**In – Standard Metal**
**Out – Standard Cell,"**
**Zvi Or-Bach, eASIC founder and CEO**


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# Structured ASIC

- **About 20 years ago**
  - **Full custom design → Standard Cell**
  - **Design cost of Full custom : $10 million**
- **Today**
  - **Standard Cell : exceeds $10 million**
- **Paradigm Shift in ASIC technology?**
  - **In – Standard Metal : Structured ASIC**
  - **Out – Standard Cell**

# ASIC development costs

Figure 1 - FPGA, cell-based ASIC, and structured ASIC development costs

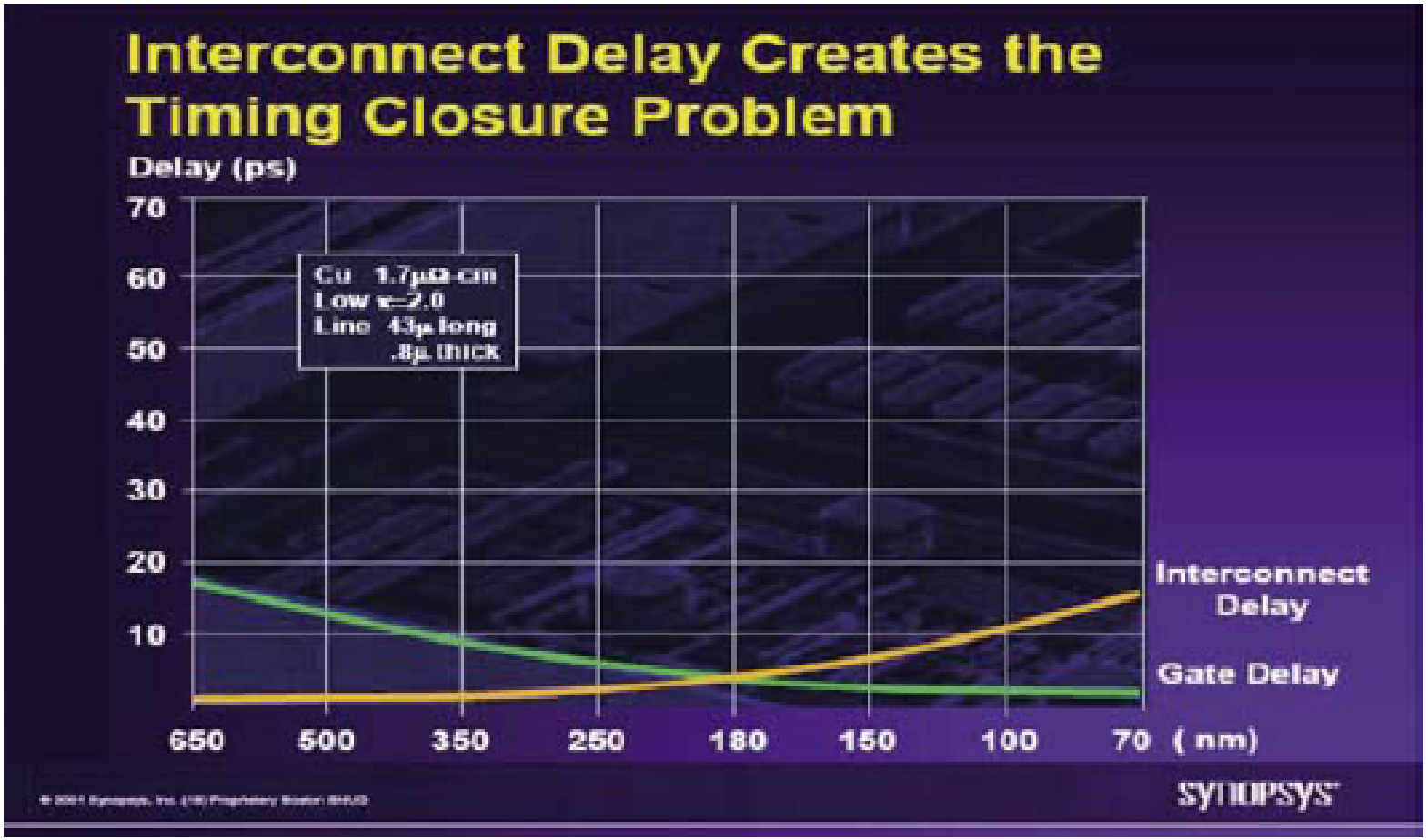
| Table 1 - Comparing Total Costs of doing in 1M gate designs in 0.13um<br>Note: Prorated Unit Cost = Per piece cost + (Qty/Total Design Cost) | | | |
|---|---|---|---|
| | FPGA | Structured ASIC | Cell-based ASIC |
| Total Design Cost: | ~$165K | ~ $500K | ~ $5.5M (Typical) |
| Vendor NRE: | None | ~ $100K - $200K | $1M to $3M |
| # Tools Required: | 2 to 3 | 2 to 3 | 6 to 10 |
| Cost of Tools: | ~ $30K | ~ $120K to $250K | > $300K<br>(# seats?) |
| # Engineers: | 1 to 2 | 2 to 3 | 5 to 7 |
| Price per chip: | $220 to $1K | ~ $30 to $150 | ~ $30 |
| Total Unit Cost<br>Qty 1K: | ~ $1000 ('03) | $500 to $650 | $ 55K |
| Total Unit Cost<br>Qty 5K: | ~ $220 (4Q'04) | $100 to $150 | $1.1K |
| Total Unit Cost<br>Qty 500K: | ~ $40 (4Q'04) | > $21 | $11 to $20 |

# Definition

- **Structured ASIC**
  - **Key to reducing design cost and complexity**
    - **Reducing number of custom mask and via layers**
    - **Typically, two or three (sometimes 5) user-modifiable metal layers**
    - **Multiple input lookup tables, F/Fs, and MUXs**

# Interconnection –Taking Over 'delay domination'

Transistors no Longer Dominate – Metal Interconnections Took Over

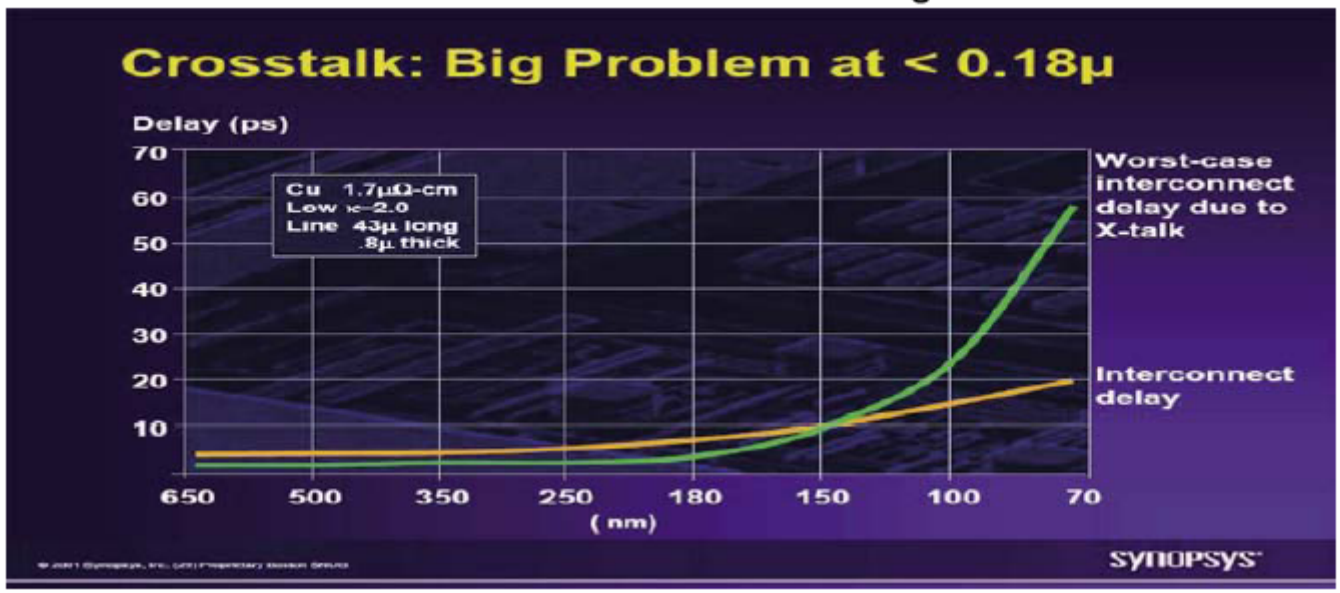


# Interconnection

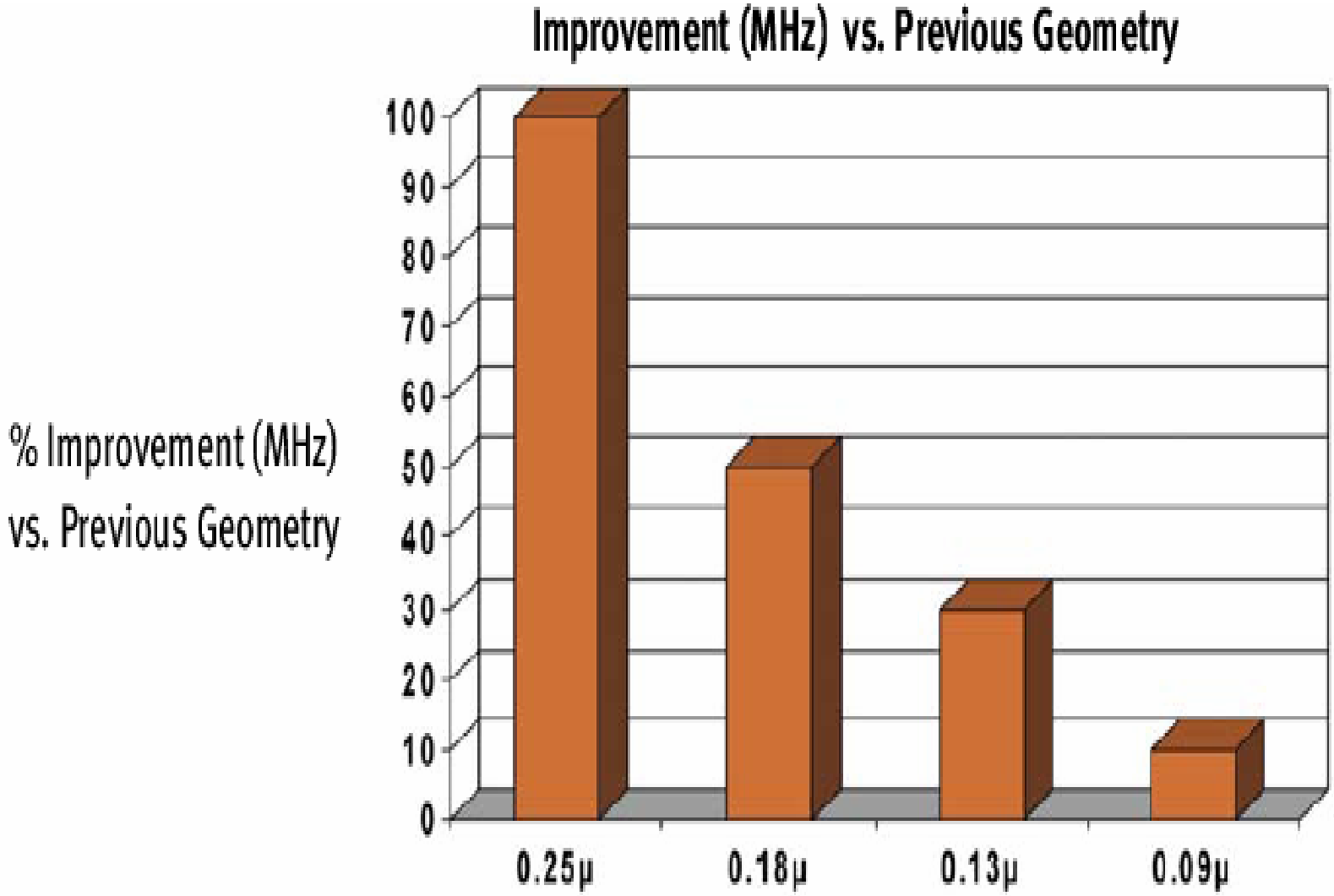
- **At 100 nm**
  - **Interconnect switching energy = TR switching energy x 3**
  - **At 35 nm, 30 times greater**

- **Crosstalk**

And Even Worse: Wire to Wire is Taking Over



# Improvement (MHz) vs. Previous Geometry



# Paradigm Shift

- **Transistor sizing (Full custom) → gate sizing (Standard Cell)**
  - **Move to an even coarser building block**
- **Immediate benefit of coarse grain cells**

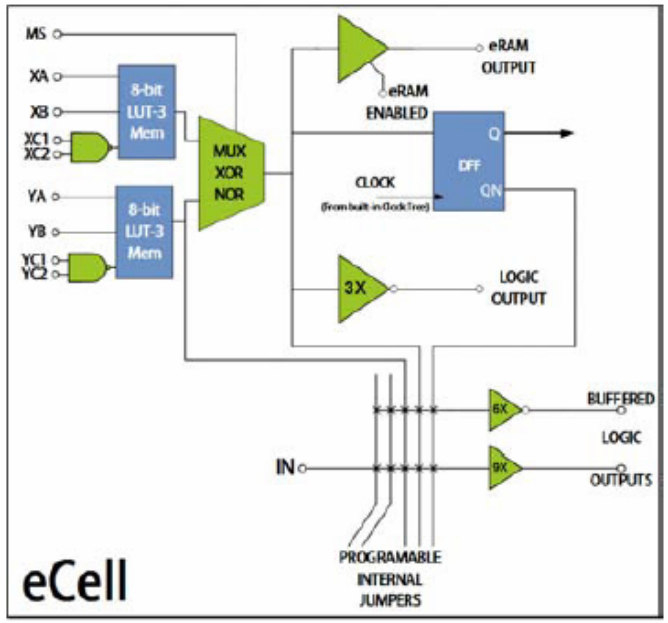
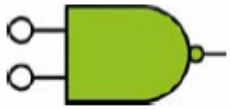


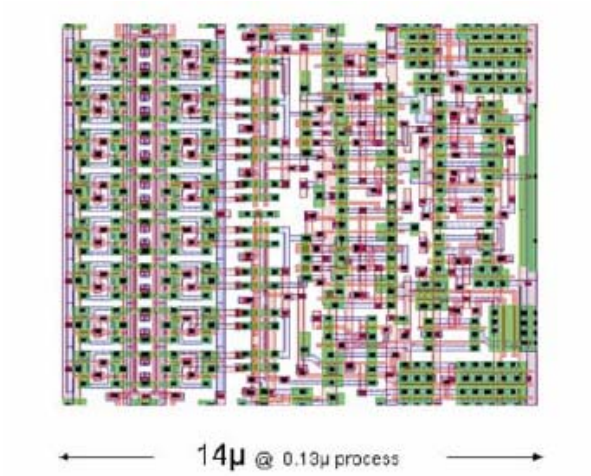

Figure 4.

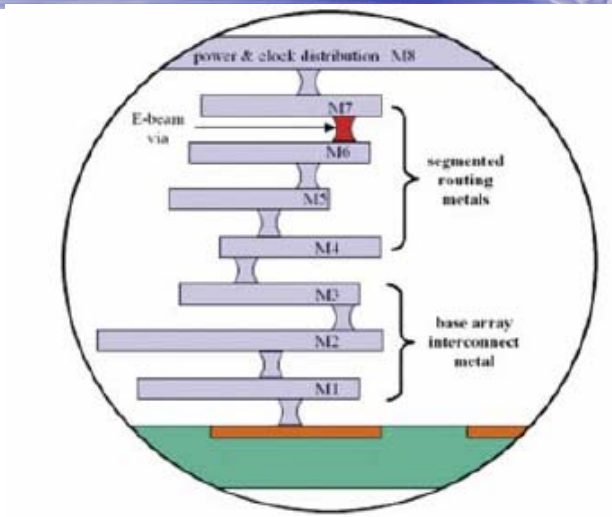
- Fine grained Standard Cell needs an average of 3 ports per gate to route
  - 3 ports, 1 gate => 3 ports/gate



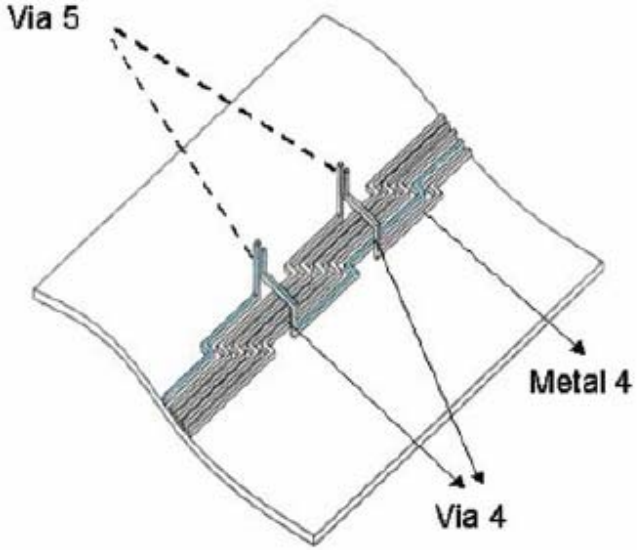
- Coarse grained eASIC/FPGA need an average of 1 port per gate to route.
  - 11 ports avg., 15 gates => ~0.75 port/gate
- **~4:1 reduction in routing needs is gained by using eASIC fabric**

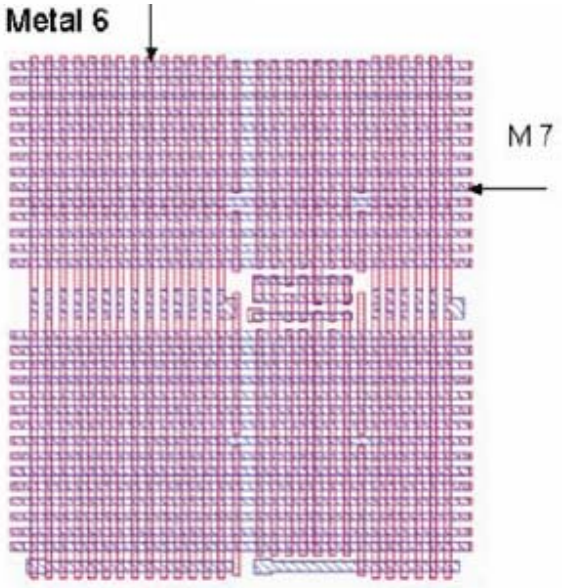
# Placement and Routing



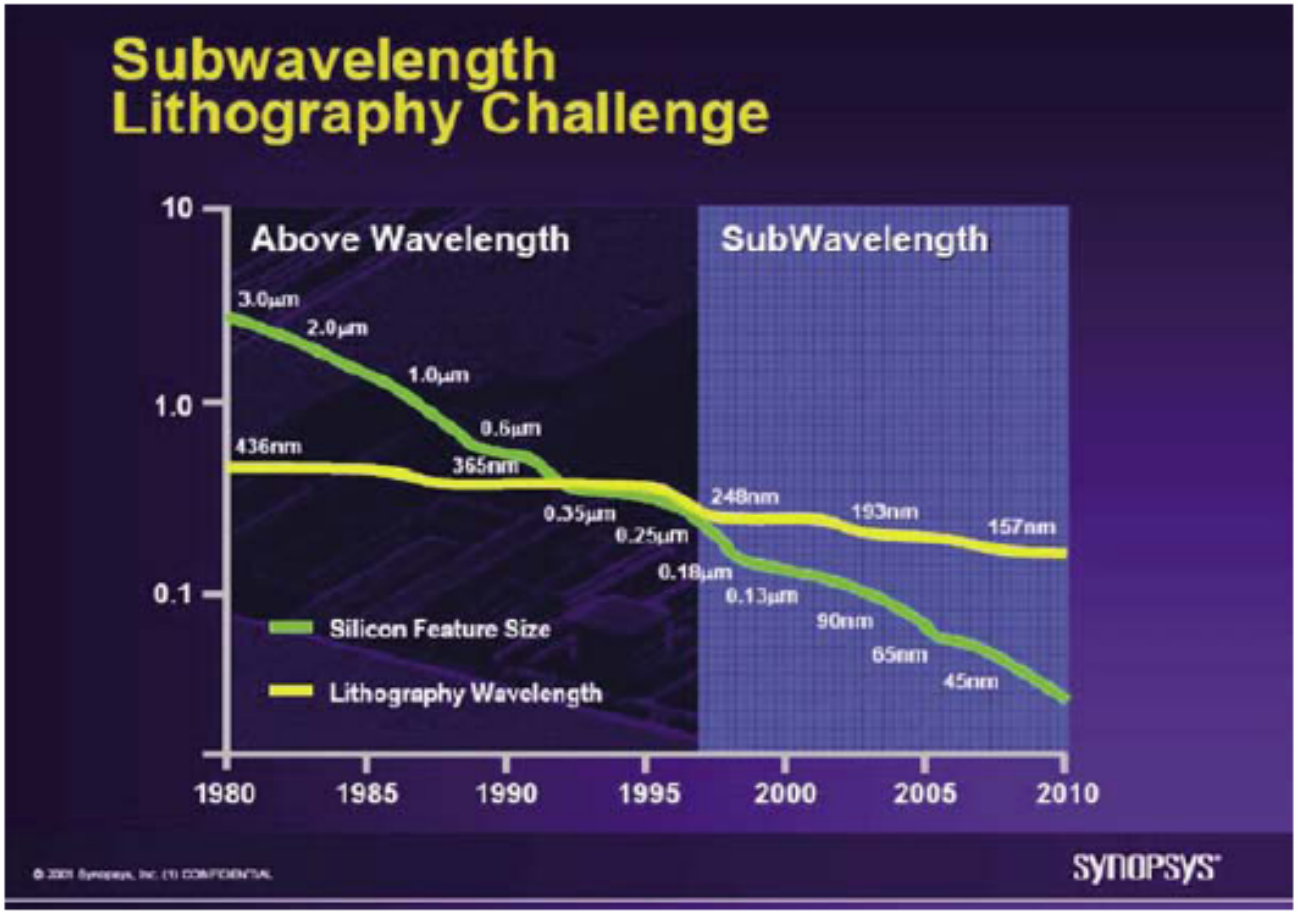




Basic Cell (14 μ)



# Feature-limited – Taking over the 'Yield Domination'



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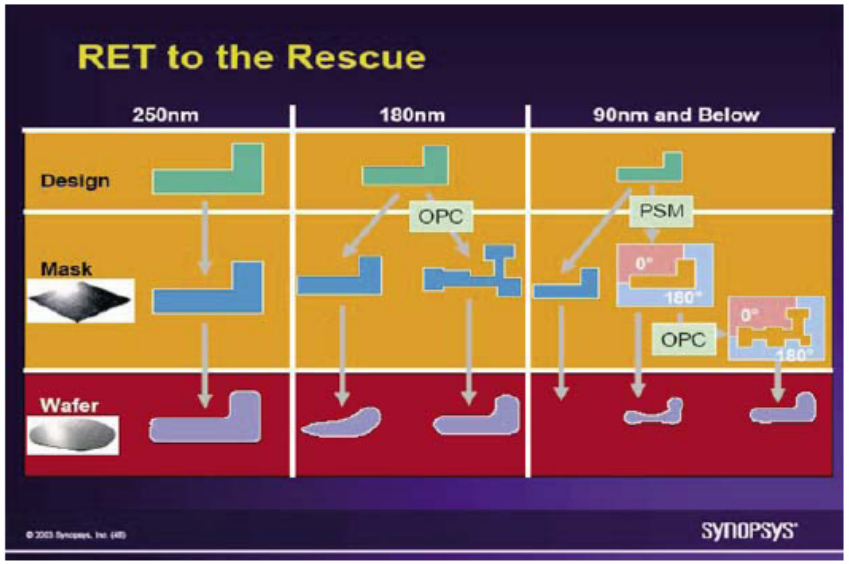
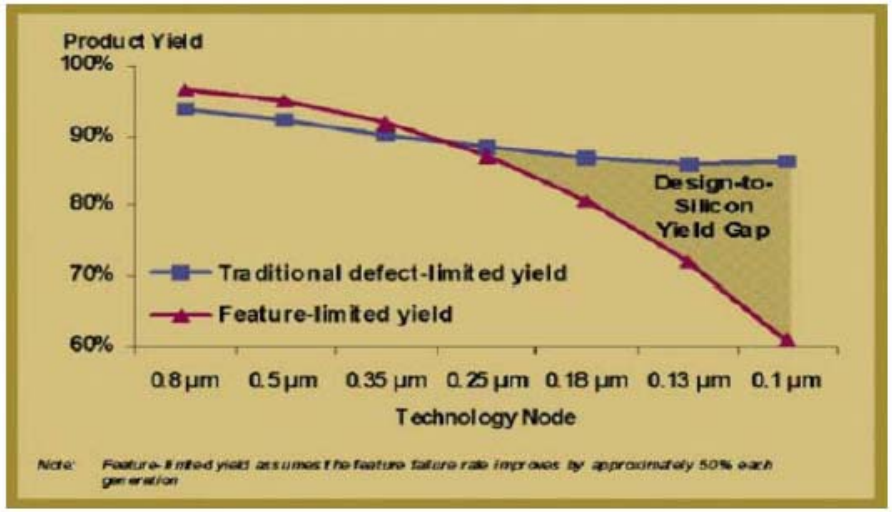



RET: Reticle Enhancement Technique

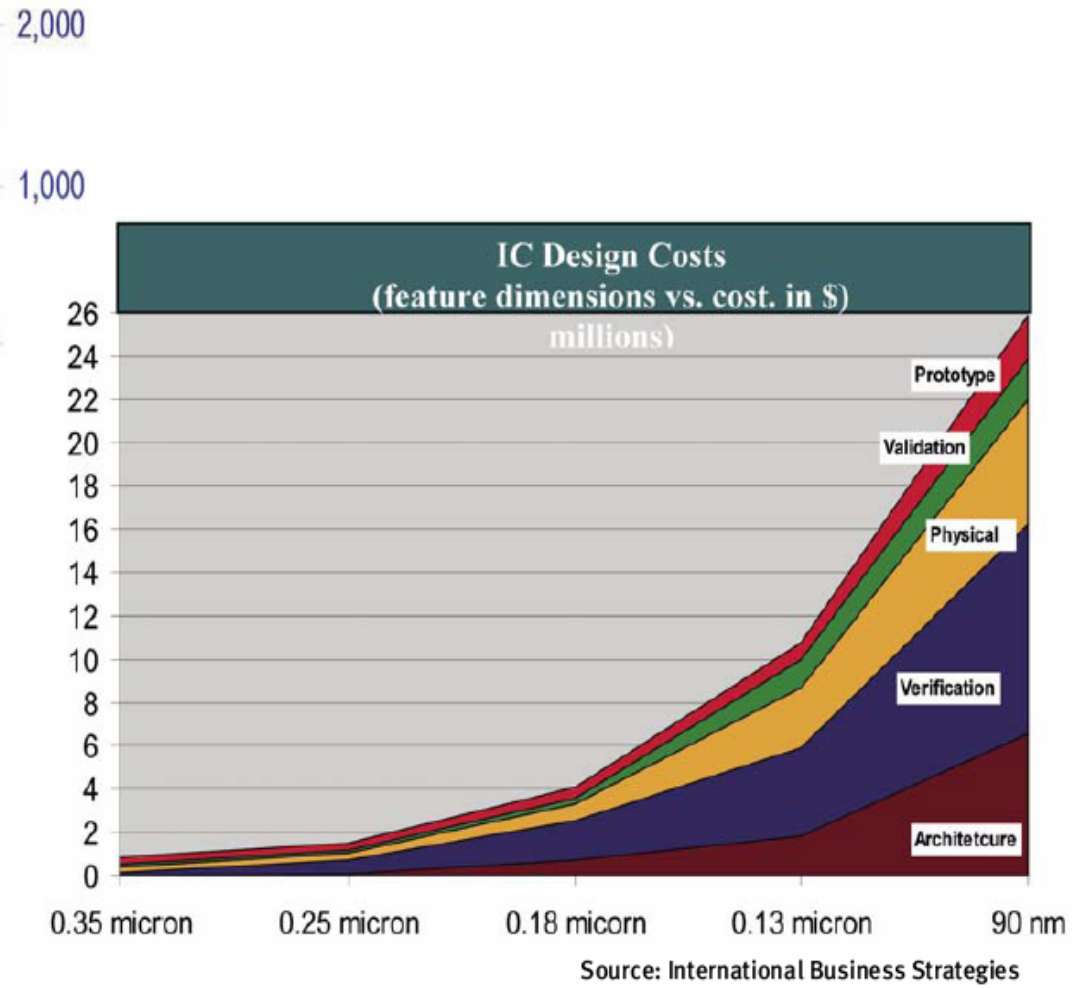



Courtesy of PDF Solutions Inc.

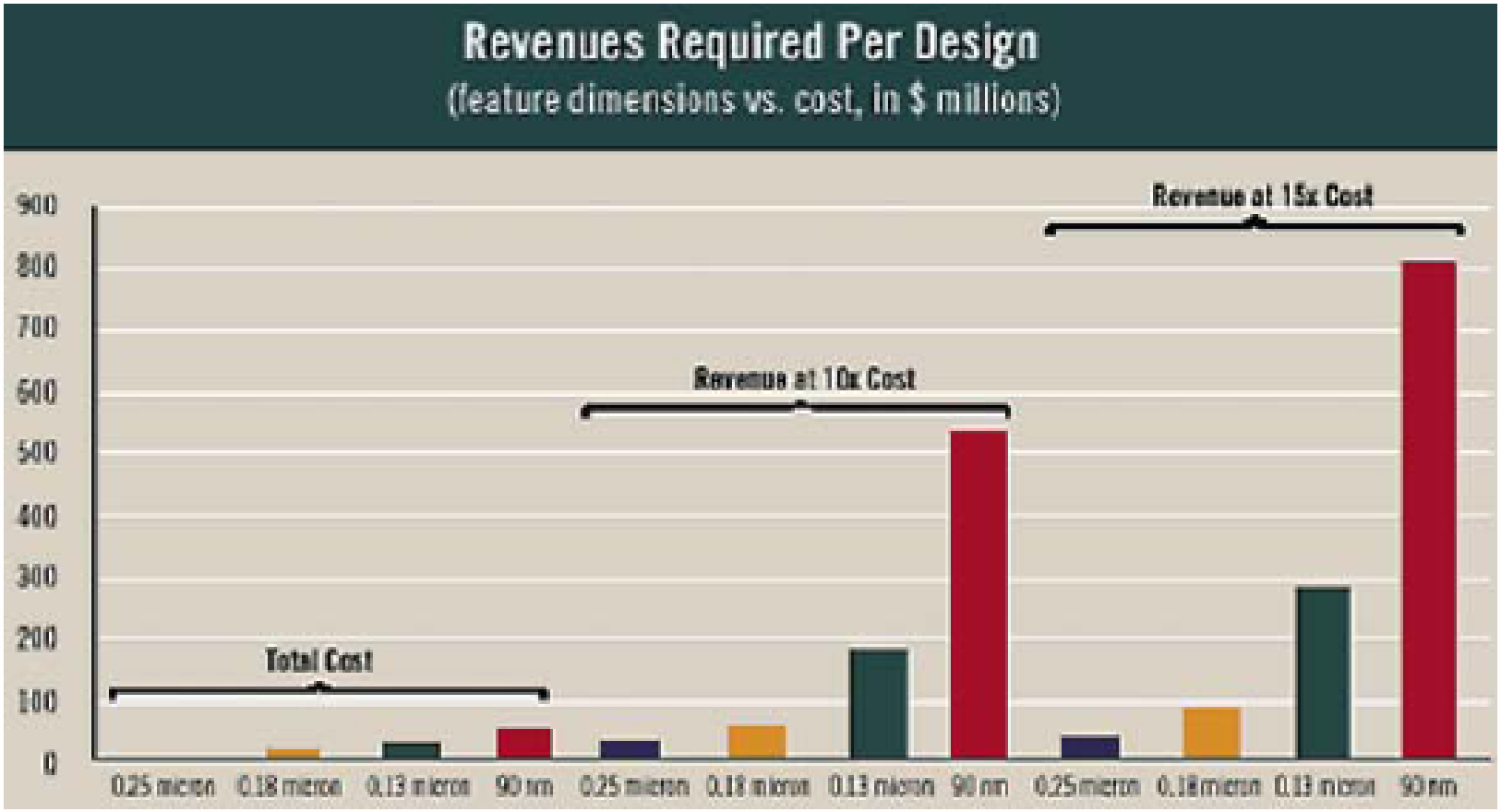
- Natural solution for this yield: use repetitive patterns, just as in SRAM

# Mask Set Cost Becomes Prohibitive

| Process (μ) | 2.0 | ... | 0.8 | 0.6 | 0.35 | 0.25 | 0.18 | 0.13 | 0.09 |
|---|---|---|---|---|---|---|---|---|---|
| Single Mask cost ($K) | 1.5 | | 1.5 | 2.5 | 4.5 | 7.5 | 12 | 40 | 60 |
| # of Masks | 12 | | 12 | 12 | 16 | 20 | 26 | 30 | 34 |
| Mask Set cost ($K) | 18 | | 18 | 30 | 72 | 150 | 312 | 1,000 | 2,000 |



# Implication of the design cost increase




Source: International Business Strategies