XC4000E CLB Characteristics Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted

CLB Switching Characteristics Guidelines

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Combinatorial Delays										
F/G inputs to X/Y outputs	T_{ILO}		2.7		2.0		1.6		1.3	ns
F/G inputs via H to X/Y outputs	T_{IHO}		4.7		4.3		2.7		2.2	ns
C inputs via SR through H to X/Y outputs	T_{HH0O}		4.1		3.3		2.4		1.9	ns
C inputs via H to X/Y outputs	T_{HH1O}		3.7		3.6		2.2		1.6	ns
C inputs via DIN through H to X/Y outputs	T_{HH2O}		4.5		3.6		2.6		1.9	ns
CLB Fast Carry Logic										
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		3.2		2.6		2.1		1.7	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		5.5		4.4		3.7		2.5	ns
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.7		1.7		1.4		1.2	ns
CIN through function generators to X/Y outputs	T_{SUM}		3.8		3.3		2.6		1.8	ns
CIN to COUT, bypass function generators	T_{BYP}		1.0		0.7		0.6		0.5	ns
Sequential Delays										
Clock K to outputs Q	T_{CKO}		3.7		2.8		2.8		1.9	ns
Setup Time before Clock K										
F/G inputs	T_{ICK}	4.0		3.0		2.4		1.8		ns
F/G inputs via H	T_{IHCK}	6.1		4.6		3.9		2.8		ns
C inputs via H0 through H	T_{HH0CK}	4.5		3.6		3.5		2.4		ns
C inputs via H1 through H	T_{HH1CK}	5.0		4.1		3.3		2.1		ns
C inputs via H2 through H	T_{HH2CK}	4.8		3.8		3.7		2.5		ns
C inputs via DIN	T_{DICK}	3.0		2.4		2.0		1.0		ns
C inputs via EC	T_{ECCK}	4.0		3.0		2.6		2.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	4.2		4.0		4.0		1.5		ns
C_{IN} input via F/G	T_{CCK}	2.5		2.1						ns
C_{IN} input via F/G and H	T_{CHCK}	4.2		3.5						ns