TABLE 3–*EDN* PLD DIRECTORY: REPRESENTATIVE EMBEDDED PROGRAMMABLE-LOGIC CORES

Product line and configuration technology (antifuse, EPROM, flash, PROM, ROM, SRAM, or other)	Core operating voltages (V)	Logic-cell count	Contents of each logic cell	LUT-derived memory density (bits)
Actel 0.18-micron VariCore EPGA IP Cores (SRAM)	1.8	1024 to 8192	Three-input LUT, register	NA
Adaptive Silicon MSA 2500 Programmable Logic Core (SRAM)	1.8 (0.18 micron), 1.3 (0.13 micron), 1 (0.10 micron)	64 to 1024	Four three-input/one-output truth tables with four registers and multiple multiplexers	NA
Agere Systems eORCA macrocell (embedded ORCA Series 4) (SRAM)	1.5	800	Eight four-input LUTs, nine registers, 10 tristate bidirectional buffers, PAL-like logic for as-much-as-10-bit decoding and AND-OR-INVERT logic	102,400
Atmel Embedded FPGA SRAM	1.8 to 3.3	256 to 6400	2×3-input LUT or four-input LUT with or without D-type register, plus multiplier AND gate, internal feedback, and tristate driver	NA

Note: Information in this table, including pricing, comes directly from the vendors. Please confirm information before finalizing your design.

Dedicated memory density (bits)	Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price range (end of 2001: 10,000 units; cheapest package; lowest speed; commercial temperature)
36,864 to 73,728 (optional)	9216		Scalable, reconfigurable, pin-fixing tool, ASIC design flow, JTAG- and BIST-interface support	Variable; combination of license and royalties
NA	NA	Carry look ahead in each cell	Fast, parallel programming, online reconfigurability, online nondestructive program-bits read-back, embedded BIST structures and program	Per-design license, plus per-part royalty
NA	NA	Boundary scan of all interface signals (except clocks), configuration logic for serial programming and read-back, including daisy-chaining of multiple eFPGAs	Fully (four sides) or partially embeddable (three sides, with one available for I/O signals) macrocell, 400 maximum signals from ASIC to eFPGA, 1280 maximum signals from eFPGA to ASIC, embedding multiple eFPGA blocks is possible	Quoted as part of ASIC design
2048 to 51,200	128		Dynamically reconfigurable at the core-cell level, very low power	NRE and licensing fees, plus per-unit cost based on silicon area