TABLE 1–REPRESENTATIVE FPGAs

Product (configuration technology)	Core operating voltages (V)	Packaging and pin-count options	Logic cells	Contents of each logic cell	LUT-derived memory-density range (bits)
Actel					
Axcelerator (antifuse)	1.5	CS 128, FBGA 256/484/676/896/1152, PBGA 729	672 to 10,752 register cells, 1344 to 21,504 combinatorial cells	Four-input multiplexer and register (register cell), three-input multiplexer, two-input AND gate, two-input OR gate, inverter (combinatorial cell)	NA
eX (antifuse)	2.5	TQFP 64/100, CSP 49/128/180	64 to 256 register cells, 128 to 512 combinatorial cells	Four-input multiplexer and register (register cell), three-input multiplexer, two-input AND gate, two-input OR gate, inverter (combinatorial cell)	NA
MX (antifuse)	3.3, 5	CQFP 208/256, PBGA 272, PLCC 44/68/84, PQFP 100/160/208/240, TQFP 176, VQFP 80/100/176	348 to 1230 register cells,295 to 1184 combinatorial cells	Three-input multiplexer and two-input OR gate (combinatorial cell)	NA
ProASIC (flash)	2.5	FBGA 144/676, PBGA 272/456, PQFP 208	5376 to 26,880	Three-input combinatorial- or sequential-logic cluster	NA
ProASIC Plus (flash)	2.5	FBGA 144/256/484/676/896/1152, PBGA 456, PQFP 208, TQFP 100	3072 to 56,320	Three-input combinatorial- or sequential-logic cluster	NA
SX (antifuse)	3.3	FBGA 144, PBGA 313/329, PLCC 84, PQFP 208, TQFP 144/176, VQFP 100	256 to 1080 register cells, 512 to 1800 combinatorial cells	Four-input multiplexer and register (register cell), three-input multiplexer, two-input AND gate, two-input OR gate, inverter (combinatorial cell)	NA
SX-A (antifuse)	2.5	CQFP 208/256, FBGA 144/256/484, PBGA 329, PQFP 208, TQFP 100/144/176	256 to 2012 register cells, 512 to 4024 combinatorial cells	Four-input multiplexer and register (register cell), three-input multiplexer, two-input AND gate, two-input OR gate, inverter (combinatorial cell)	NA
Altera					
Acex 1K (SRAM)	2.5V	F 256/484, Q 208, T 100/144	576 to 4992	Four-input LUT, register, programmable carry chain, programmable cascade chain	NA
Apex 20K (SRAM)	2.5	1-mm BGA, 1.27-mm BGA, PQFP, RQFP, TQFP (144 pins to 672 pins)	4160 to 16,640	Four-input LUT, register, programmable carry chain, programmable cascade chain	NA
Apex 20KC (SRAM)	1.8	1-mm BGA, 1.27-mm BGA, PQFP, RQFP (208 to 1020 pins)	8320 to 38,400	Four-input LUT, register, programmable carry chain, programmable cascade chain	NA
Apex 20KE (SRAM)	1.8	1-mm BGA, 1.27-mm BGA, PQFP, RQFP, TQFP (144 to 1020 pins)	1200 to 51,840	Four-input LUT, one register, programmable carry chain, programmable cascade chain	NA
Apex II (SRAM)	1.5	B 724, F 672/1020/1508	16,640 to 67,200	Four-input LUT, register, programmable carry chain, programmable cascade chain	NA
Excalibur EPXA (SRAM)	1.8	FBGA 484/672/1020	4160 to 38,400	Four-input LUT, register, programmable carry chain, programmable cascade chain	NA

Dedicated memory-density range (bits)	Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price (10,000 units, end of 2002, cheapest package, lowest speed, commercial temperature)
29,440 to 338,688	4608	FIFO controllers, per-pin FIFOs, eight PLLs	Single-chip, nonvolatile, secure, live at power-up, fouor debugging probes	$124 (AX1000)
NA	NA	NA	Single-chip, nonvolatile, secure	$2.30 (eX64)
2560 (MX 36 only)	256 (MX 36 only)	NA	Single-chip, nonvolatile, secure, also available in military-temperature- and 883B-qualified versions	$2.90 (A40MX02)
13,824 to 64,512	2304	Dedicated FIFO-control logic	Single-chip, nonvolatile, secure, reprogrammable, ASIC-design flow, also available in industrial-temperature versions	$12.20 (A500K050)
14,336 to 64,512	2304	Dedicated FIFO-control logic, PLL, LVPECL I/O buffers	Single-chip,nonvolatile, secure, reprogrammable, in-system programmable, live at power-up, ASIC-design flow	$14 (APA075)
27,648 to 202,752	NA	NA	Single-chip; nonvolatile; secure; also available in military-temperature, 833B-qualified, e-flow, and radiation-tolerant versions	$7.50 (A54SX08)
NA	NA	NA	Single-chip, nonvolatile, secure, also available in military-tempeature and 833B-qualified versions	$4.40 (A54SX08A)
12,228 to 49,152	4096	Logic-array blocks, embedded array blocks, general-purpose PLL	In-circuit reconfiguration, multivolt-I/O support, JTAG and boundary-scan-test support, 64-bit and 66-MHz PCI compliance, support for Nios embedded processor	$5 to $17
53,248 to 212,992	2048	Logic-array blocks, embedded system blocks, PLL, MegaLabs	LVTTL, LVCMOS, and PCI support; in-circuit reconfiguration; multivolt-I/O support; JTAG and boundary-scan-test support; support for Nios embedded processor	$27 to $185
106,496 to 327,680	2048	Copper interconnect, two to four PLLs, 840-Mbps LVDS I/O buffers, logic-array blocks, embedded system blocks, MegaLabs, SignalTap embedded logic analyzer	I/O standards support for SSTL, PCI, GTL+, AGP, CTT, LVPECL, LVCMOS, and LVTTL; in-circuit reconfiguration; multivolt-I/O support; JTAG and boundary-scan-test support; support for Nios embedded processor	$60 to $405
24,576 to 442,368	2048	Two to four PLLs, 840-Mbps LVDS I/O buffers, logic-array blocks, embedded system blocks, MegaLabs SignalTap, embedded logic analyzer	I/O standards support for SSTL, PCI, GTL+, AGP, CTT, LVPECL, LVCMOS, and LVTTL; in-circuit reconfiguration; multivolt-I/O support; JTAG and boundary scan test support; support for Nios embedded processor	$11 to $450
425,984 to 1,146,880	4096	Copper interconnect, four PLLs, eight global clocks, 1-Gbps I/O buffers, logic-array blocks, embedded system blocks, MegaLabs, SignalTap embedded logic analyzer	I/O standards support for HyperTransport, SSTL, PCI, GTL+, AGP, CTT, LVPECL, LVCMOS, and LVTTL; multivolt-I/O support; JTAG and boundary-scan-test support; support for Nios embedded processor	$160 to $1070
53,248 to 327,680	2048	ARM922T processor, UART, timer, SDR/DDR SDRAM controller, 32 to 256 kbytes of SRAM, 16 to 128 kbytes of dual-port SRAM, interrupt controller, AMBA/AHB1 and AHB2 buses, expansion-bus interface, FPGA-configuration logic, embedded trace (ETM9) module, JTAG and APEX 20KE-like FPGA fabric	186 to 711 user I/Os; advanced I/O support; 1.8, 2.5, or 3.3V I/Os; 26 to 160 embedded system blocks; content-addressable-memory support; processor operates independently of the FPGA; support for Nios embedded processor	$40 to $750

TABLE 1–REPRESENTATIVE FPGAs (con't)

Product (configuration technology)	Core operating voltages (V)	Packaging and pin-count options	Logic cells	Contents of each logic cell	LUT-derived memory-density range (bits)
Altera (con't)					
Mercury (SRAM)	1.8	1-mm BGA (484 to 780 pins)	4800 to 14,400	Four-input LUT, register, programmable carry chain, programmable cascade chain	NA
Stratix (SRAM)	1.5	1-mm BGA, 1.27-mm BGA (672 to 1923 pins)	10,570 to 114,140	Four-input LUT, register, programmable carry chain, programmable cascade chain	NA
Atmel					
AT6000 (SRAM)	3.3, 5	BQFP 132, PLCC 84, PQFP 208/240, TQFP 144, VQFP 100	1024 to 6400	Seven-input multiplexer, three two-input AND gates, two-input XOR gate, D-type register, two inverters	NA
AT40K (SRAM)	3.3, 5	LQFP144, PLCC84, PQFP100/160/240, PQFP304, SBGA352, TQFP100, VQFP208	256 to 2304	Two three-input lookup tables, 15-input multiplexer, two-input AND gate, D-type register, three-state buffer	4096 to 36,864
AT94K (SRAM)	3.3	PLCC84, TQFP100/144, VQFP208	256 to 2304	Two three-input lookup tables, 15-input multiplexer, two-input AND gate, D-type register, three-state buffer	4096 to 36,864
AT94S (SRAM)	3.3	CABGA 256	256 to 2304	Two three-input lookup tables, 15-input multiplexer, two-input AND gate, D-type register, three-state buffer	4096 to 36,864
Lattice ispXPGA	1.5, 2.5, 3.3	FPBGA 900, FPSBGA 680	1936 to 15,376	Four four-input LUTs, four configurable sequential elements, wide logic generator	1936 to 15,376
ORCA2	3.3, 5	BGA 272, PBGA 388, PLCC 84, PQFP 160/208/240/304, SBGA 432, TQFP 100/144	100 to 900	Four four-input LUTs, four configurable sequential elements, wide logic generator	6400 to 57,600
ORCA3C	5	PBGA 272, PQFP 208/240	484	Eight four-input LUTs, eight latches or registers, additional register	61,952
ORCA3L	2.5	PBGA 388, PQFP 208/240, SBGA 432/600	1024 to 1444	Eight four-input LUTs, eight latches or registers, additional register	131,072 to 184,832
ORCA3T	3.3	PQFP 208/240/272/388, SBGA 432/600	144 to 784	Eight four-input LUTs, eight latches or registers, additional register	18,432 to 100,352
ORCA4E	1.5	FPBGA 416/680, PBGA 388	624 to 2024	Eight four-input LUTs, eight latches or registers, additional register	79,872 to 259,072
ORLI10G	1.5	FPBGA 680	1296	Eight four-input LUTs, eight latches or registers, additional register	165,888
ORT82G5	1.5	FPBGA 680	1296	Eight four-input LUTs, eight latches or registers, additional register	165,888

Dedicated memory-density range (bits)	Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price (10,000 units, end of 2002, cheapest package, lowest speed, commercial temperature)
49,152 to 114,688	4096	Two to four PLLs, four global clocks, 1.25-Gbps clock-and-data-recovery transceivers, LVDS I/O buffers, logic-array blocks, embedded system blocks, MegaLabs, SignalTap embedded logic analyzer, quad-port RAM	Carry-select look-ahead mode, multiplier mode, multivolt-I/O operation, in-circuit reconfiguration, JTAG and boundary-scan-test support, I/O-row bands, array-driver technology, support for Nios embedded processor	$100 to $230
920,448 to 10,118,016	512, 4,096, or 524,288	12 PLLs, 40 global clocks, 840-Mbps LVDS I/O buffers, DSP blocks, Trimatrix memory, terminator technology, array logic-blocks, MegaLabs, SignalTap embedded logic analyzer	Copper interconnects; I/O standards support for HyerTransport, SSTL, PCI, GTL+, AGP, CTT, LVPECL, LVCMOS, PCML, HSTL and LVTTL; multivolt-I/O support; JTAG and boundary-scan-test support; support for Nios embedded processor	$100 to $1600
NA	NA	NA	Partial and dynamic reconfiguration	$15 to $70
2048 to 18,432	128	Registers in I/O buffers	Partial and dynamic reconfiguration, PCI compliant, core-cell direct connections	$3 to $90
2048 to 18,432	128	Registers in I/O buffers, 8-Bit AVR microcontroller and 36 kbytes of program and data SRAM	Partial and dynamic reconfiguration, PCI compliant, 16 internal interrupts, 16 IO-select lines, two UARTs, three timer/counters, 8×8-bit hardware multiplier, four external interrupts, two-wire interface peripheral	$5 to $65
2048 to 18,432	128	Registers in I/O buffers, 8-Bit AVR microcontroller and 36 kbytes of program and data SRAM, 256 kbit to 1 Mbit of configuration EEPROM	Partial and dynamic reconfiguration, PCI compliant, 16 internal interrupts, 16 IO-select lines, two UARTs, three timer/counters, 8×8-bit hardware multiplier, four external interrupts, two-wire interface peripheral	$10 to $85
92,160 to 414,720	4096	System memory, system-clock PLL, system HSI serializer/deserializer	Nonvolatile, instant-on and reconfigurable, no external memory required, as many as 496 user I/Os, system-IO multistandard configuration, IEEE 1532- and IEEE1149.1-compliant	$45 to $345
NA	NA	NA	As many as 43,200 usable logic gates, as many as 480 user I/Os, register and latch options, PCI-bus compliance, boundary-scan IEEE 1149.1 JTAG	$8.48 to $105
NA	NA	NA	18,600 usable logic gates, as many as 298 user I/Os, as many as four Express-clock inputs, boundary-scan IEEE 1149.1 JTAG	$102
NA	NA	NA	As many as 340,000 usable logic gates, as many as 442 user I/Os, 3.3V I/O supply voltage, as many as four Express-clock inputs, boundary-scan IEEE 1149.1 JTAG	$102 to $291
NA	NA	NA	As many as 18,600 usable logic gates, as many as 448 user I/Os, as many as four Express-clock inputs, boundary-scan IEEE 1149.1 JTAG	$13.66 to $128
73,728 to 147,456	9216	Eight PLLs (T1/E1, STS-3), microprocessor-unit interface, AMBA bus	200,000 to 600,000 usable logic gates; as many as 466 user I/Os; support for multiple I/O standards, including HSTL, SSTL, and GTL+; embedded quad-port RAM blocks; twin-quad programmable-function units; boundary-scan IEEE 1149.1 JTAG	$59 to $212
110,592	9216	Microprocessor-unit interface, AMBA bus	400,000 usable logic gates; support for XGMII and XSBI; support for multiple I/O standards, including HSTL, SSTL, and GTL+; bandwidth as high as 12.5 Gbps; 33, 64B/66B encoding/decoding; boundary-scan IEEE 1149.1 JTAG	$250
110,592	9216	Eight 3.125-Gbps serializer/deserializer (dual-XAUI), microprocessor interface, AMBA bus	400,000 usable logic gates; 3.125-Gbps serializer/deserializer; support for multiple I/O standards, including HSTL, SSTL, and GTL+; 8B/10B encoding/decoding; alignment FIFOs; embedded quad-port RAM blocks; twin-quad programmable-function units; boundary-scan IEEE 1149.1 JTAG	$250

TABLE 1–REPRESENTATIVE FPGAs (con't)

Product (configuration technology)	Core operating voltages (V)	Packaging and pin-count options	Logic cells	Contents of each logic cell	LUT-derived memory-density range (bits)
Atmel (con't)					
ORT8850H, ORT8850L	1.5	FPBGA 680	624 to 2024	Eight four-input LUTs, eight latches or registers, additional register	79,872 to 259,072
QuickLogic					
Eclipse (antifuse)	2.5	FPBGA 0.8-mm 280, 1-mm 484 and 672, 1.27-mm 516, PQFP 208	960 to 4032	Two six-input AND gates, four two-input AND gates, seven two-input multiplexers, two registers, as many as six independent outputs	NA
EclipsePlus (antifuse)	2.5	FPBGA 0.8-mm 280, 1-mm 484 and 672, 1.27-mm 516, PQFP 208	960 to 4032	Two six-input AND gates, four two-input AND gates, seven two-input multiplexers, two registers, as many as six independent outputs	NA
pASIC1 (antifuse)	5	PLCC 44/68, TQFP 100/144	64 to 180	Two six-input AND gates, four two-input AND gates, three two-input multiplexers, register, as many as five independent outputs	NA
pASIC2 (antifuse)	3.3, 5	PBGA 256, PLCC 84, PQFP 208, TQFP 100/144	192 to 672	Two six-input AND gates, four two-input AND gates, three two-input multiplexers, register, as many as five independent outputs	NA
pASIC3 (antifuse)	3.3	PBGA 256/456, PLCC 68/84, PQFP 208, TQFP 100/144/208	96 to 1584	Two six-input AND gates, four two-input AND gates, three two-input multiplexers, register, as many as five independent outputs	NA
QuickFC (antifuse)	3.3	PBGA 456, PQFP 208	560	Two six-input AND gates, four two-input AND gates, three two-input multiplexers, register, as many as five independent outputs	NA
QuickMIPS (antifuse)	5	PBGA 680	2016	Two six-input AND gates, four two-input AND gates, seven two-input multiplexers, two registers, as many as six independent outputs	NA
QuickPCI (antifuse)	3.3	PBGA 256, 456, 484, 516; PQFP 208; TQFP 144	266 to 1427	Two six-input AND gates, four two-input AND gates, seven two-input multiplexers, two registers, as many as six independent outputs	NA
QuickRAM (antifuse)	3.3	CQFP 256,456, 484; PQFP 208; TQFP 144	160 to 1302	Two six-input AND gates, four two-input AND gates, three two-input multiplexers, register, as many as five independent outputs	NA
QuickSD (antifuse)	2.5	0.8-mm FPBGA 280, 1-mm 484, 672; 1.27-mm 516; PQFP 208	2016	Two six-input AND gates, four two-input AND gates, three two-input multiplexers, register, as many as five independent outputs	NA
Triscend					
A7 CSoC (SRAM)	2.5	BGA 324, 484; PQFP 208	512 to 3200	Four-input LUT, D-type flip-flop with clock enable and asynchronous set or reset, carry/cascade logic, connections to internal address/data bus, debugging logic, optional look-up-table configuration as 8-bit serial-in/serial-out shift register	8192 to 51,200

Dedicated memory-density range (bits)	Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price (10,000 units, end of 2002, cheapest package, lowest speed, commercial temperature)
73,728 to 147,456	9216	Eight 850-Mbps serializer/deserializer, microprocessor interface, AMBA bus	200,000 or 600,000 usable logic gates; pseudo-SONET framing; supports GTL+, PECL, SSTL3/2, HSTL, and LVDS I/O standards; embedded quad-port RAM blocks; twin-quad programmable-function units; boundary-scan IEEE 1149.1 JTAG	$128 to $350
As much as 82,944	NA	NA	600-MHz internal speeds, advanced clock capability, programmable I/O buffers	$12 to $70
40,080 to 82,944	NA	NA	600-MHz internal speeds, advanced clock capability, programmable I/O buffers	$13 to $77
NA	NA	NA	Faster-than-400-MHz performance, 100% routability and reliability	$10 to $40
NA	NA	NA	Faster-than-400-MHz performance, 100% routability and reliability	$12 to $50
NA	NA	NA	Faster-than-400-MHz performance, 100% routability and reliability	$4 to $25
25,344	NA	Fibre Channel ENDEC	Data-transfer rates as high as 2.5 Gbps for proprietary links	$38
82,944	2304	MIPS Technologies MIPS32 4Kc processor; AHB and APB buses with peripherals; two 10/100 Ethernet ports; 32-bit, 33- or 66-MHz PCI host; on-chip debugging blocks	Hardware/software co-design with system-development kit, in-system analyzer, and system mode	$60
11,500 to 50,690	NA	32- or 64-bit, 33- 66-, or 75-MHz master/target PCI controller	As much as 600-Mbyte/sec bus performance with zero wait states, reference-design kits with boards, devices, and software drivers	$9 to $50
As much as 25,344	NA	NA	600-MHz internal speeds, advanced clock capability, programmable I/O buffers	$5 to $35
82,944	2304	Bus LVDS transceivers	Serial data-transfer rates as high as 5 Gbps, conversion rates of 1-to-1 to 1-to-10	$40
131,072	131,072	ARM7TDMI 32-bit RISC processor, 8-kbyte unified cache, barrel shifter, hardware multiplier, Thumb extensions, debugging extensions, local-CPU bus, external SRAM and SDRAM interfaces, four-channel DMA controller, two 16C450/550-style UARTs with modem, two 16-bit timer/counters, 32-bit watchdog timer, interrupt controller, multi-master high-speed internal bus, 32 to 200 address decoders, power management, power-on reset, hardware breakpoint unit, JTAG port, internal ring oscillator, crystal-oscillator amplifier, registers in I/O buffers, selectable output-drive current	Supported from ARM-based development tools and RTOS environments, pin-compatible package footprint among family members, 2.5 or 3.3V I/O buffers, ASIC-based cost-reduction path available	$19.95 (A7S20)

TABLE 1–REPRESENTATIVE FPGAs (con't)

Product (configuration technology)	Core operating voltages (V)	Packaging and pin-count options	Logic cells	Contents of each logic cell	LUT-derived memory-density range (bits)
Triscend (con't)					
E5 CSoC (SRAM)	3.3	BGA 484, LQFP 128, PQFP 208	256 to 3200	Four-input LUT, D-type flip-flop with clock enable and asynchronous set or reset, carry/cascade logic, connections to internal address/data bus, debugging logic, optional look-up-table configuration as 8-bit serial-in/serial-out shift register	4096 to 51,200
Xilinx					
Spartan II	2.5	CS 144; FG 256, 456; PQ 208; TQ 144; VQ 100	432 to 5292	Four-input function generator, carry logic, register	6144 to 75,264
Spartan IIE	1.8	FG 456, FT 256, PQ 208, TQ 144	1728 to 6912	Four-input function generator, carry logic, register	24,576 to 98,304
Virtex-II	1.5	BF 957; BG 575, 728; CS 144, FF 896, 1152, 1517 676; FG 256, 456,	576 to 104,882	Four-input LUT, register, carry logic	8192 to 1,490,944
Virtex-II Pro	1.5	FF2 676, 896, 1152, 1148, 1517, 1696, 1704; FG 256/456	3168 to 125,136	Four-input LUT, register, carry logic	45,056 to 1,779,712

Dedicated memory-density range (bits)	Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price (10,000 units, end of 2002, cheapest package, lowest speed, commercial temperature)
65,536 to 524,288	65,536 to 524,288	Accelerated 8051/8052-compatible, 8-bit microcontroller; three 16-bit timer/counters; UART; watchdog timer; interrupt controller; two-channel DMA controller; external memory interface; multimaster high-speed internal bus; 16 to 200 address decoders; power management; power-on reset; hardware breakpoint unit; JTAG port; internal ring oscillator; crystal-oscillator amplifier; registers in I/O buffers; selectable output-drive current	Supported from 8051/8052 compilers and debuggers, pin-compatible package foot-print among family members, 5V-tolerant I/O buffers, ASIC-based cost-reduction path available	$4.80 to $18.75
16,384 to 57,344	4096	Four DLLs, dedicated carry logic for high-speed arithmetic, low-skew global clock nets, registers in I/O buffers	Fully PCI compliant, IEEE 1149.1-compatible boundary-scan logic	$6.55 to $19.45
32,768 to 65,536	4096	19 high-performance interface standards, including LVDS and LVPECL; as many as 120 differential-I/O pairs; four DLLs; dedicated carry logic for high-speed arithmetic; low-skew global clock nets; registers in I/O buffers	Fully PCI compliant, IEEE 1149.1-compatible boundary-scan logic	$9.50 to $29.95
73,728 to 3,096,576	18,432	As many as 168 18×18-bit multipliers, as many as 12 digital-clock managers, XCITE digitally controlled impedance technology, TripleDES security	0.5-trillion-multiply-accumulate DSP performance; 840-Mbps LVDS on any pin pair; BLVDS, LVPECL, HSTL I, II, III, IV, SSTL 2 and 3, PCI, PCI 64/66, and PCI-X support; SRL16 allows shift registers as large as 128 bits in one configurable-logic block	XC2V40: $14 to XC2V8000: $3900
221,184 to 10,248,192	18,432	As many as four PowerPC405 cores, as many as 24 3.125-Gbps transceivers, as many as 556 18×18-bit multipliers, as many as 12 digital-clock managers, XCITE digitally controlled impedance technology, TripleDES security	1-trillion-multiply-accumulate DSP performance; transceiver support for Infiniband, RapidIO Serial, Serial ATA, and 3GIO; differential signaling with 840-Mbps LVDS on any pin pair; BLVDS, LVPECL, single-ended connectivity with HSTL I, II, III, IV, SSTL 2 and 3, PCI and PCI 64/66; SRL16 allows shift registers as large as 128 bits in one configurable-logic block	XC2VP2: $40, XC2VP100: $3200, XC2VP125: $5000

TABLE 2–REPRESENTATIVE PALs, SPLDs AND CPLDs

Product (configuration technology)	Core operating voltages (V)	Packaging and pin-count options	Logic cells	Contents of each logic cell	LUT-derived memory-density range (bits)	Dedicated memory-density range (bits)
Altera						
MAX 3000 (EEPROM)	3.3	0.8-mm BGA, PLCC, PQFP, TQFP (44 to 208 pins)	32 to 512	16/36	Global	NA
MAX 7000AE (EEPROM)	3.3	0.8-mm BGA, 1-mm BGA, 1.27-mm BGA, PLCC, PQFP, TQFP (44 to 256 pins)	32 to 512	16/36	Global	NA
MAX 7000B (EEPROM)	2.5	0.8-mm BGA, 1-mm BGA, 1.27-mm BGA, PLCC, PQFP, TQFP (44 to 256 pins)	32 to 512	16/36	Global	NA
MAX 7000S (EEPROM)	5	PLCC, PQFP, RQFP, TQFP (44 to 208 pins)	32 to 256	16/36	Global	NA
Anachip						
PEEL array (EEPROM)	4.75 to 5.25	DIP 24/28/40, PLCC 28/44, SOIC 24/28, TQFP 44, TSSOP 28	40 to 72	As many as 80 inputs/block	Global	NA
PEEL device (EEPROM)	4.75 to 5.25	DIP20/24, PLCC 20/28, SOIC 20/24, TSSOP 20/24	Eight to 10	As many as 22 inputs/block	Global	NA
TPLD (tiny programmable-logic device) (EEPROM)	3	PDIP 8, SIP 8, SOIC 8, TSOP 8	10	As many as 32 inputs/block	Global	NA
Zero-power PEEL device (EEPROM)	2.7 to 3.6, 4.75 to 5.25	DIP 20/24, PLCC 20/28, SOIC 20/24, TSSOP 20/24	Eight to 10	As many as 22 inputs/block	Global	NA
Atmel						
ATF15xxAE (EEPROM)	3.3	BGA 49/100/256, PLCC 44/68/84, PQFP 100/160/208, TQFP 44/100/144	32 to 512	16/40	Global	NA
ATF15xxAS (EEPROM)	5	PLCC 4468/84, PQFP 100/160, TQFP44/100	32 to 128	16/40	Global	NA
ATF15xxASV (EEPROM)	3.3	PLCC 4468/84, PQFP 100/160, TQFP44/100	32 to 128	16/40	Global	NA
ATF15xxSE (EEPROM)	5	BGA 49/100/256, PLCC 44/68/84/100, PQFP 160/208, TQFP44/100/144	32 to 256	16/40	Global	NA
ATF16LV8C, ATF22-LV10C (EEPROM)	3.3 to 5	DIP 20/24, PLCC 20/28, SOIC 20/24, TSSOP 20/24	Eight to 10	NA	Global	NA
ATF16V8B, ATF20-V8B (EEPROM)	5	PDIP 20/24, PLCC 20/28, SOIC 20/24, TSSOP 20/24	Eight to 10	NA	Global	NA
ATF16V8C, ATF20-V8C, ATF22V10C (EEPROM)	5	DIP 20/24, PLCC 20/28, SOIC 20/24, TSSOP 20/24	Eight to 10	NA	Global	NA
ATF2500B (EPROM)	5	DIP 40, LCC 44, PLCC 44	24	NA	Global	NA
ATF2500C (EEPROM)	5	DIP 40, LCC 44, PLCC 44	24	NA	Global	NA
ATF750C, ATF750-LVC (EEPROM)	3.3, 5	DIP 24, PLCC 28, SOIC 24, TSSOP 24	10	NA	Global	NA
Cypress Semiconductor						
2.5-Gbps tranceivers	3.3	BGA 456	1536	16/36	Hierarchical	245,760
Delta39K (SRAM)	1.8 to 3.3	FBGA 256/484/676, PQFP 208, Self-Boot BGA 388, Self-Boot FBGA 256/484/676	512 to 3072	16/36	Hierarchical	81,920 to 491,520

Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price (10,000 units, end of 2002, cheapest package, lowest speed, commercial temperature)
NA	NA	2.5, 3.3, 5V-compatible I/O; 4.5-nsec propagation delays; low-power mode; FAST programming times; JTAG in-system-programmable support; PCI compatible	$1 to $8
NA	NA	2.5, 3.3, 5V-compatible I/O; 4.5-nsec propagation delays; low-power mode; FAST programming times; JTAG in-system-programmable support; PCI compatible	$1.40 to $29
NA	NA	1.8, 2.5, 3.3V-compatible I/O; support for GTL+ and SSTL I/O standards; 3.5-nsec propagation delays; low-power mode; JTAG in-system-programmable support; PCI compatible	$1.40 to $29
NA	NA	3.3 and 5V-compatible I/O, 6-nsec propagation delays, low-power mode, JTAG in-system-programmable support, PCI compatible	$3 to $34
NA	NA	NA	$2.41 to $2.86
NA	NA	NA	39 cents to 99 cents
NA	Schmitt trigger, programmable clock, programmable clock polarity	NA	50 cents to 75 cents
NA	Schmitt trigger on all inputs, including clock	NA	$1.30 to $1.63
NA	NA	Input-transition detection on L versions	90 cents to $15
NA	NA	Input-transition detection on L versions	$1 to $4
NA	NA	Input-transition detection on L versions	$1 to $4
NA	NA	Input-transition detection on Z versions	90 cents to $8
NA	NA	Quarter-power Q versions, input-transistion detection on QL and Z/QZ versions	50 cents to 90 cents
NA	NA	Quarter-power Q versions, input-transistion detection on QL versions	40 cents to 55 cents
NA	NA	Quarter-power Q versions, input-transistion detection on QL and Z/QZ versions	65 cents to 85 cents
NA	NA	Quarter-power Q versions, input-transistion detection on QL and Z/QZ versions	$2.50
NA	NA	Quarter-power Q versions, input-transistion detection on QL and Z/QZ versions	$2.50
NA	NA	Input-transistion detection on QL and Z/QZ versions	90 cents to $1
4096 (channel) and 8192 (cluster)	Integrated 2.5-Gbps serializer/ deserializer, clock- and data-recovery unit, clock-multiplier unit, postamplifier	Infiniband-compliant, low jitter, low power, self-boot	$75
4096 (channel) and 8192 (cluster)	Spread-spectrum-aware PLL; built-in FIFO and dual-port arbitration logic; two registers in each I/O cell, support for multiple I/O standards, including PCI, GTL+, SSTL, HSTL, QDR; carry-chain logic	Zero-power, self-boot, Compact PCI hot-swap compatible, JTAG	$17 to $65

TABLE 2–REPRESENTATIVE PALs, SPLDs AND CPLDs (con't)

Product (configuration technology)	Core operating voltages (V)	Packaging and pin-count options	Logic cells	Contents of each logic cell	LUT-derived memory-density range (bits)	Dedicated memory-density range (bits)
Cypress Semiconductor (con't)						
HOTLink II	3.3	BGA 456	1536	16/36	Hierarchical	245,760
OC-48 serializer/ deserializer	3.3	BGA 456	1536	16/36	Hierarchical	245,760
Quantum38K (SRAM)	2.5 to 3.3	FBGA 256/484, PQFP 208	512 to 1536	16/36	Hierarchical	16,384 to 49,152
Ultra37000 (EEPROM)	3.3 to 5	BGA 256/352, CLCC 44/84, CQFP 160/208, PLCC 44/84, PQFP 208, TQFP 44/100/160	32 to 512	16/36	Global	NA
Lattice Semiconductor						
16V8 (EEPROM)	3.3, 5	PDIP 20, PLCC 20	Eight	NA	Global	NA
20V8 (EEPROM)	3.3, 5	PDIP 24, PLCC 28	Eight	NA	Global	NA
22V10 (EEPROM)	3.3, 5	PDIP 24, PLCC 28	10	NA	Global	NA
ispGAL22V10 (EEPROM)	3.3, 5	PLCC 28, SSOP 28	10	NA	Global	NA
ispLSI 5000VE (EEPROM)	3.3	BGA 272/388, FPBGA 256/388, TQFP 100/128	128 to 512	32/68	Global	NA
ispMACH 4000B, 4000C, 4000V (EEPROM)	18, 2.5, 3.3	FPBGA 256, TQFP 44/48/ 100/128/176	32 to 512	16/36	Global	NA
ispMACH4A (EEPROM)	3.3, 5	BGA 256, CABGA 100, FPBGA 144/256/388, PLCC 44, PQFP 100/208, TQFP 44/48/100/144	32 to 512	16/36	Global	NA
ispMACH 5000B (EEPROM)	2.5	FPBGA 256/484, PQFP 208, TQFP 128	128 to 512	32/68	Global	NA
ispMACH 5000VG (EEPROM)	3.3	FPBGA 256/484/676	768 to 1024	32/68	Hierachical	NA
ispXPLD 5000MX (EEPROM)	18, 2.5, 3.3	FPBGA 256/484/672, PQFP 208	256 to 1024	32/68	Global	131,072 to 524,288 (use subtracts from available logic resources)
STMicroelectronics						
PSD4235G2/V (flash)	3.3, 5	TQFP 80	16	NA	Global	4,194,304
PSD4256G6V (flash)	2.7	TQFP 80	16	NA	Global	8,388,608
PSD835G2/V (flash)	3.3, 5	TQFP 80	16	NA	Global	4,194,304
PSD8XXF2/V (flash)	3.3, 5	PLCC 52, PQFP 52	16	NA	Global	1,048,576 to 2,097,152
Xilinx						
CoolRunner-II (EEPROM)	1.8	CP 56/132, FG 324, FT 256, PC 44, PQ 208, TQ 144, VQ 44/100	32 to 512	16/56	Global	NA

Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price (10,000 units, end of 2002, cheapest package, lowest speed, commercial temperature)
4096 (channel) and 8192 (cluster)	Four 0.2- to 1.5-Gbps serial links, 8B/10B encoding, channel bonding, 100,000 gates	GbE, FC, ESCON, DVB, SMPTE-compliant, redundant I/Os, self-boot	$80
4096 (channel) and 8192 (cluster)	Integrated OC-48/STM-16 serializer/deserializer, clock- and data-recovery unit, clock-multiplier unit, postamplifier	Gigabit Ethernet-, Fibre Channel-, ESCON-, DVB-, SMPTE-compliant; redundant I/Os; self-boot	$140
4,096	Built-in dual-port arbitration logic, two registers in each I/O cell, carry-chain logic	Compact PCI hot-swap compatible, JTAG	$12.50 to $23
NA	Dedicated input pins with two registers	In-system reprogrammable, 16 product terms per macrocell, JTAG, programmable bus hold	$1 to $30
NA	NA	3.5-nsec propagation delay	90 cents to $3.45
NA	NA	3.5-nsec propagation delay	$1.11 to $9.03
NA	NA	4-nsec propagation delay	$2.10 to $13.46
NA	NA	4-nsec propagation delay, in-system programmable	$3.68 to $7.65
NA	NA	5-nsec propagation delay, 180-MHz speed, IEEE 1149.1-scan testable, in-system programmable	$9.25 to $11.75
NA	NA	1.8, 2.5, and 3.3V I/O support; 2.5-nsec propagation delay; 400-MHz speed; IEEE 1149.1-scan testable; in-system programmable via IEEE 1532 I²C-compliant interface	$3.10 to $43.25
NA	NA	5-nsec propagation delay, 182-MHz speed, IEEE 1149.1-scan testable, in-system programmable	$1 to $78.75
NA	NA	System I/O support for standards, including HSTL, SSTL, GTL+, and LVCMOS; 3.5-nsec propagation delay; 275-MHz speed; IEEE 1149.1-scan testable; in-system programmable via IEEE 1532 I²C-compliant interface	$13.85 to $54.50
NA	System-clock PLL	SuperBIG logic density; system-clock PLL timing control; system-I/O support for standards, including HSTL, SSTL, GTL+, and LVCMOS; as many as 160 product terms per output; 5-nsec propagation delay; 178-MHz speed; IEEE 1149.1-scan testable; in-system programmable via IEEE 1532 I²C-compliant interface	$67.50 to $97
16,384 (use subtracts from available logic resources)	Flexible multifunction block, system-clock PLL	Each multifunction block is programmable as logic, RAM, FIFO, or content-addressable memory; system-clock PLL timing control, system-I/O support for standards, including HSTL, SSTL, GTL+, and LVCMOS; low power; 3.5-nsec propagation delay; 285-MHz speed; IEEE 1149.1-scan testable; ispXP in-system programmable and reconfigurable	$9.75 to $36.95
524,288	Dual flash memories, 64-kbit SRAM, 52 I/O pins, programmable microprocessor-unit interface	In-system programmable via JTAG	$6.73
1,048,576	Dual flash memories, 256-kbit SRAM, 52 I/O pins, programmable microprocessor-unit interface	In-system programmable via JTAG	$8.21
524,288	Dual flash memories, 64-kbit SRAM, 52 I/O pins, programmable microprocessor-unit interface	In-system programmable via JTAG	$6.73
131,072 to 262,144	Dual flash memories, as much as 256 kbits of SRAM, 27 I/O pins, programmable microcontroller-unit interface	In-system programmable via JTAG	$4.29
NA	Clock doubler, clock divider, Cool clock, HSTL/SSTL support	High performance, ultralow standby power, advanced design security, input hysteresis	$1.15 to $39.50

TABLE 3–REPRESENTATIVE EMBEDDED PROGRAMMABLE LOGIC CORES

Product (configuration technology)	Core operating voltages (V)	Logic cells	Contents of each logic cell	LUT-derived memory-density range (bits)	Dedicated memory-density range (bits)
Actel					
0.13-micron VariCore EPGA (SRAM)	1.2	1024 to 8192	Three-input look-up table, register	NA	36,864 to 147,456 (optional)
0.18-micron VariCore EPGA (SRAM)	1.8	1024 to 8192	Three-input look-up table, register	NA	36,864 to 73,728 (optional)
Atmel					
Embedded FPGA (SRAM)	1.8 to 3.3	256 to 6400	Two three-input look-up tables or a four-input LUT with optional D-type register plus multiplier AND gate, internal feedback, three-state driver	NA	2048 to 51,200
Leopard Logic					
Hyperlink CCL (SRAM)	Process-dependent, supports TSMC 0.18- and 0.13-micron, others on request	256 to 4096	Four-input LUT; support for five- and six-input LUTs; two registers; carry logic; support for eight-input AND, OR, and XOR gates	NA	NA

Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price (10,000 units, end of 2002, cheapest package, lowest speed, commercial temperature)
9216	NA	Scalable, reconfigurable, pin-fixing capability, RTL input, VariCore compiler tool, ASIC-design flow, JTAG- and built-in-self-test-interface support	Nonrecurring-engineering and licensing fees, plus per-unit cost based on silicon area
9216	NA	Scalable, reconfigurable, pin-fixing capability, RTL input, VariCore compiler tool, ASIC-design flow, JTAG- and built-in-self-test-interface support	Nonrecurring engineering and licensing fees, plus per-unit cost based on silicon area
128	NA	Dynamically reconfigurable at the core cell level, low power	Nonrecurring engineering and licensing fees, plus per-unit cost based on silicon area
NA	BIST, configuration loader, configuration monitor, JTAG	Fast process porting, support for standard ASIC tools	Nonrecurring engineering and licensing fees, plus per-unit cost based on silicon area